DSC2041FI1-F0025

Crystal-less™ Configurable Clock Generator

General Description

The DSC2041FI1-F0025 is a programmable, high performance dual output oscillator utilizing Microchip's proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The Two outputs are controlled by separate supply voltages to allow for independent voltage level control. The frequencies of the outrputs can be identical or independently derived from a common PLL frequency source.

The DSC2041FI1-F0025 has provision for up to eight user-defined pre-programmed, pin-selectable output frequency combinations. DSC2041FI1-F0025 is also equipped with independent pin-selectable output drive strength for LVCMOS output to reduce EMI and noise.

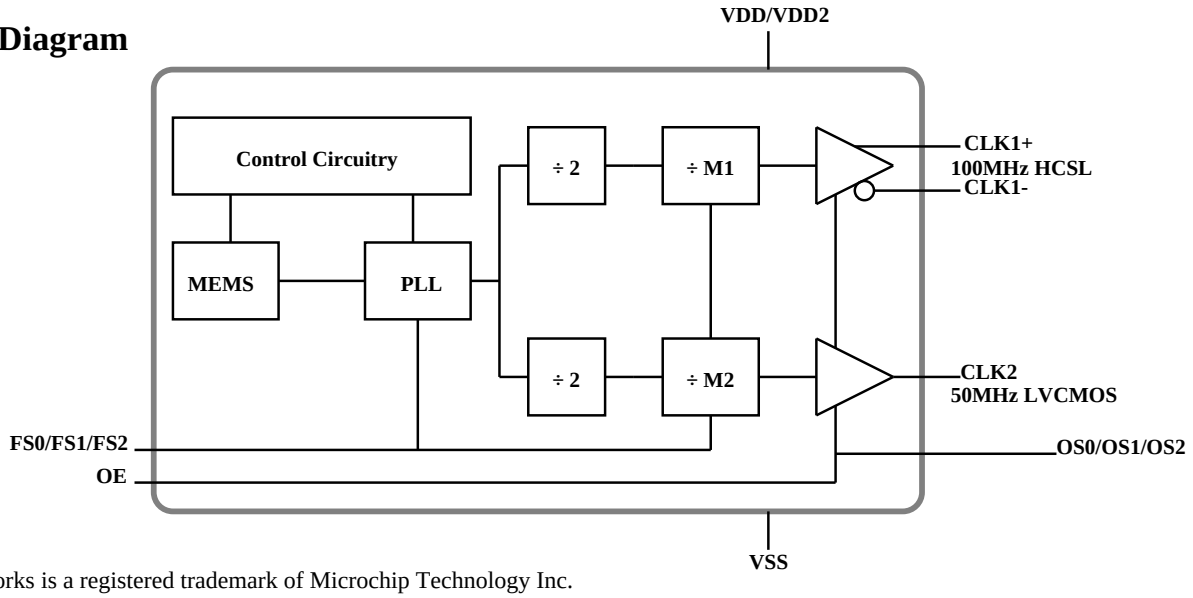
Applications

- Consumer Electronics
- Storage Area Networks
  - SATA, SAS, Fibre Channel
- Passive Optical Networks
  - EPON, 10G-EPON, GPON, 10G-GPON
- Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express
- Automotive

Features

- Frequency and output formats:
  - HCSL
    100MHz
  - LVCMOS
    50MHz
- Low RMS phase jitter: <1ps (typ)
- ±50ppm frequency stability
- -40°C to +85°C industrial temperature range
- High supply noise rejection: -50dBc
- Pin-selectable configurations
  - 3-bit output drive strength (LVCMOS)
  - Up to 8 output frequency combinations
- Excellent shock & vibration immunity
  - Qualified to MIL-STD-883
- High reliability
  - 20x better MTF than quartz oscillators
- Supply range of 2.25 to 3.6V
- AEC-Q100 automotive qualified
- 14-pin 3.2mm x 2.5mm QFN package

Block Diagram



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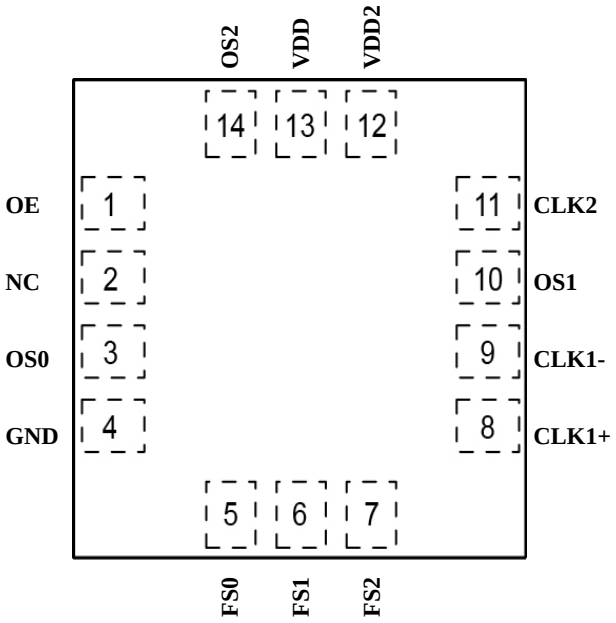
Ordering Information

Ordering Part Number	Industrial Temperature Range	Shipping	Package
DSC2041FI1-F0025	-40°C to +85°C	Tube	14-pin 3.2mm x 2.5mm QFN
DSC2041FI1-F0025T	-40°C to +85°C	Tape and Reel	14-pin 3.2mm x 2.5mm QFN

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



14-pin 3.2mm x 2.5mm QFN

Pin Description

Pin Number	Pin Name	Pin Type	Pin Function
1	OE	I	Enables outputs when high and disables outputs when low
2	NC		Leave unconnected or connect to ground
3	OS0	I	Least significant bit for output drive strength selction for LVCMOS, see Table 1 for details
4	GND	PWR	Ground
5	FS0	I	Least significant bit for frequency selection, see Table 2 for details
6	FS1	I	Middle bit for frequency selection, see Table 2 for details
7	FS2	I	Most significant bit for frequency selection, see Table 2 for details
8	CLK1+	O	Positive HCSL output
9	CLK1-	O	Negative HCSL output
10	OS1	I	Middle bit for output drive strength selection for LVCMOS, see Table 1 for details
11	CLK2	O	LVCMOS output
12	VDD2	PWR	Power supply for LVCMOS output CLK2, 1.65V to 3.6V (VDD2 ≤ VDD)
13	VDD	PWR	Power supply
14	OS2	I	Most significant bit for output drive strength selection for LVCMOS, see Table 1 for details

Operational Description

The DSC2041FI1-F0025 is a dual oscillator with an HCSL output and an LVCMOS output. The device consists of a MEMS resonator and a supporting PLL IC. The two outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL. Two constraints are imposed on the output frequencies: 1) f2 = M x f1/N, where M and N are even integers between 4 and 254, 2) 1.2GHz < N x f2 < 1.7GHz.

The actual frequencies output by DSC2041FI1-F0025 are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to eight different frequency combinations. Three control pins (FS0 - FS2) select the output frequency combination.

The DSC2041FI1-F0025 provides control of the output voltage levels of the LVCMOS output.

VDD2 (pin 12) sets the high voltage level of CLK2. VDD2 must be equal to or less than VDD at all times to insure proper operation. VDD2 can be as low as 1.65V. When OE (pin 1) is floated or connected to VDD, DSC2041FI1-F0025 is in operational mode. Driving OE to ground will tri-state both output drivers (hi-impedance mode).

The DSC2041FI1-F0025 has programmable output drive strength for LVCMOS output. Using three control pins (OS0 - OS2), the drive strength for LVCMOS output (CLK2) can be adjusted to match circuit board impedances to reduce power supply noise, overshoot/undershoot and EMI.

Table 1 displays typical rise / fall times for the output with a 15pF load capacitance as a function of these control pins at VDD = 3.3V and room temperature.

	Output Drive Strength Bits [OS2, OS1, OS0] - Default is [111]							
	000	001	010	011	100	101	110	**111**
tr (ns)	2.1	1.7	1.6	1.4	1.3	1.3	1.2	**1.1**
tf (ns)	2.5	2.4	2.4	2	1.8	1.6	1.3	**1.3**

Table 1. Rise/Fall Times for Drive Strengths

Output Clock Frequencies

Frequency select bits are weakly tied high so if left unconnected the default setting will be [111] and the device will output the associated frequency highlighted in bold.

Freq (MHz)	**Freq Select Bits [FS2, FS1, FS0] - Default is [111]**							
	000	001	010	011	100	101	110	**111**
CLK1	NA	NA	NA	NA	NA	NA	NA	**100**
CLK2	NA	NA	NA	NA	NA	NA	NA	**50**

Table 2. Pin-Selectable Output Frequencies

Absolute Maximum Ratings

Item	**Min.**	**Max.**	**Units**	**Condition**
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	VDD + 0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

1000+ years of data retention on internal memory

Specifications (Unless specified otherwise: T = 25°C, max LVCMOS drive strength)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage[1]	VDD		2.25		3.6	V
Supply Current	IDD	OE pin low - output is disabled		21	23	mA
Supply Current[2]	IDD	OE pin high - outputs are enabled HCSLL: RL = 50Ohms, F01 = 125MHz LVCMOS: CL = 15pF, F02 = 75MHz		49		mA
Frequency Stability	△F	Includes frequency variation due to initial tolerance, temp. and power supply voltage			±50	ppm
Aging	△F	First year (@ 25°C)			±5	ppm
Startup Time[3]	tSU	T = 25°C			5	ms
Input Logic Levels Input Logic High Input Logic Low	 VIH VIL		 0.75 x VDD -		 - 0.25 x VDD	V
Output Disable Time[4]	tDA				5	ns
Output Enable Time	tEN				20	ns
Pull-Up Resistor[2]		Pull-up exists on all digital IO		40		kOhms
HCSL Output						
Output Logic Levels Output Logic High Output Logic Low	 VOH VOL	RL = 50Ohms	 0.725 -		 - 0.1	V
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition Time[4] Rise Time Fall Time	 tR tF	 20% to 80% RL = 50Ohms, CL = 2pF	 200		 400	ps
Frequency	CLK1	[FS2, FS1, FS0] = [1, 1, 1]		100		MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter[5]	JPER	F01 = F02 = 156.25MHz		2.8		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 156.25MHz 100kHz to 20MHz @ 156.25MHz 12kHz to 20MHz @ 156.25MHz		0.25 0.37 1.7	 2	psRMS
LVCMOS Output						
Output Logic Levels Output Logic High Output Logic Low	 VOH VOL	 I = ±6mA	 0.9 x VDD -		 - 0.1 x VDD	V
Output Transition Time[4] Rise Time Fall Time	 tR tF	 20% to 80% CL = 15pF		 1.1 1.3	 2 2	 ns
Frequency	CLK2	[FS2, FS1, FS0] = [1, 1, 1]		50		MHz
Output Duty Cycle	SYM		45		55	%
Period Jitter[5]	JPER	F01 = F02 = 125MHz		3		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz		0.3 0.38 1.7	 2	psRMS

1. Pin 12 VDD2, and pin 13 VDD should be filtered with 0.1uF capacitors.
2. Output is enabled if OE pin is floated or not connected.
3. tSU is time to 100ppm stable output frequency after VDD is applied and outputs are enabled.
4. Output Waveform and Test Circuit figures below define the parameters.
5. Period Jitter includes crosstalk from adjacent output.

Nominal Performance Parameters (Unless specified otherwise: T = 25°C, VDD = 3.3V)

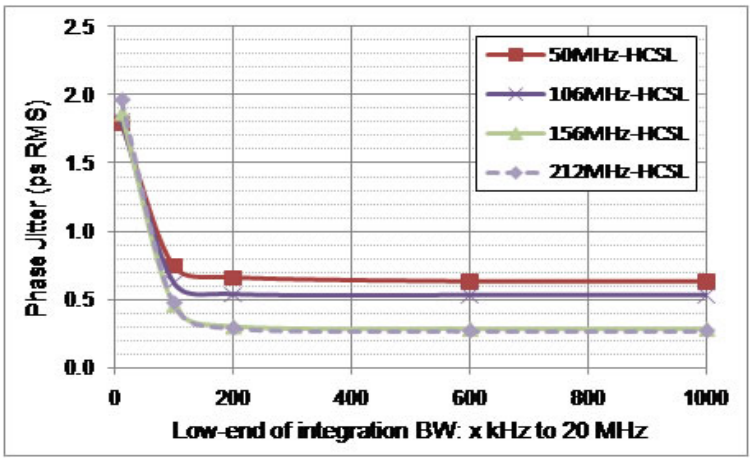


Figure 1. HCSL Phase Jitter (integrated phase noise)

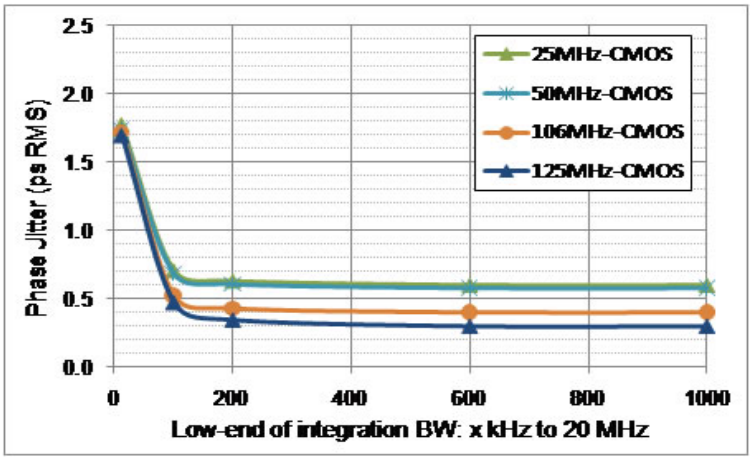


Figure 2. LVCMOS Phase Jitter (integrated phase noise)

HCSL Output Waveform

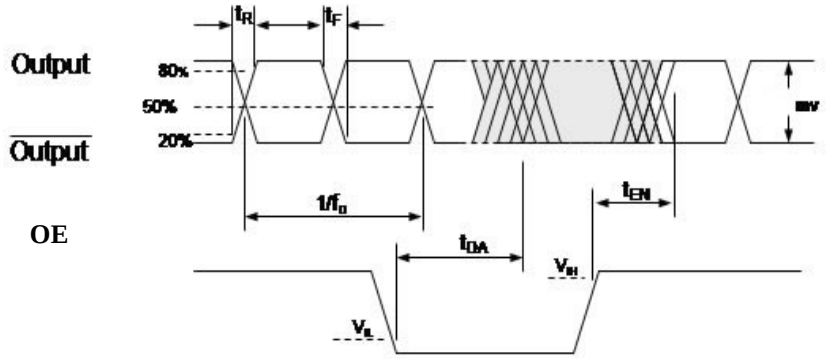


Figure 3. HCSL Output Waveform

LVCMOS Output Waveform

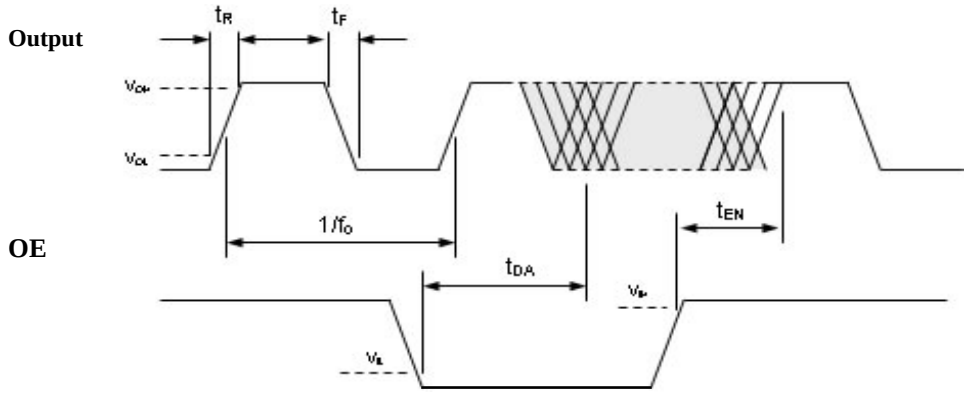


Figure 4. LVCMOS Output Waveform

MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec Max.
Preheat Time 150°C to 200°C	60 - 180 sec
Time maintained above 217°C	60 - 150 sec
Peak Temperature	255 - 260°C
Time within 5°C of actual Peak	20 - 40 sec
Ramp-Down Rate	6°C/sec Max.
Time 25°C to Peak Temperature	8 min Max.

Solder Reflow Profile

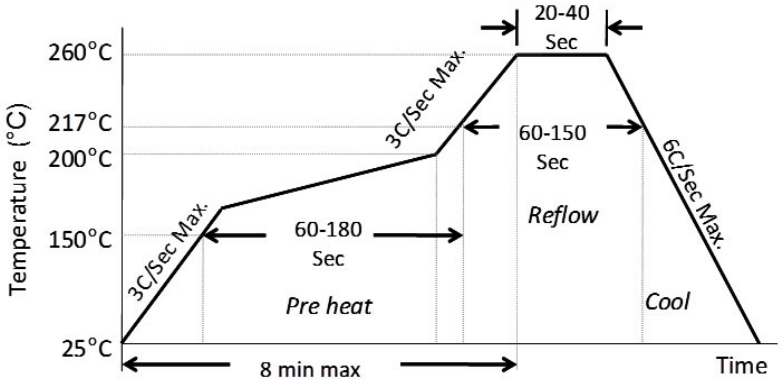
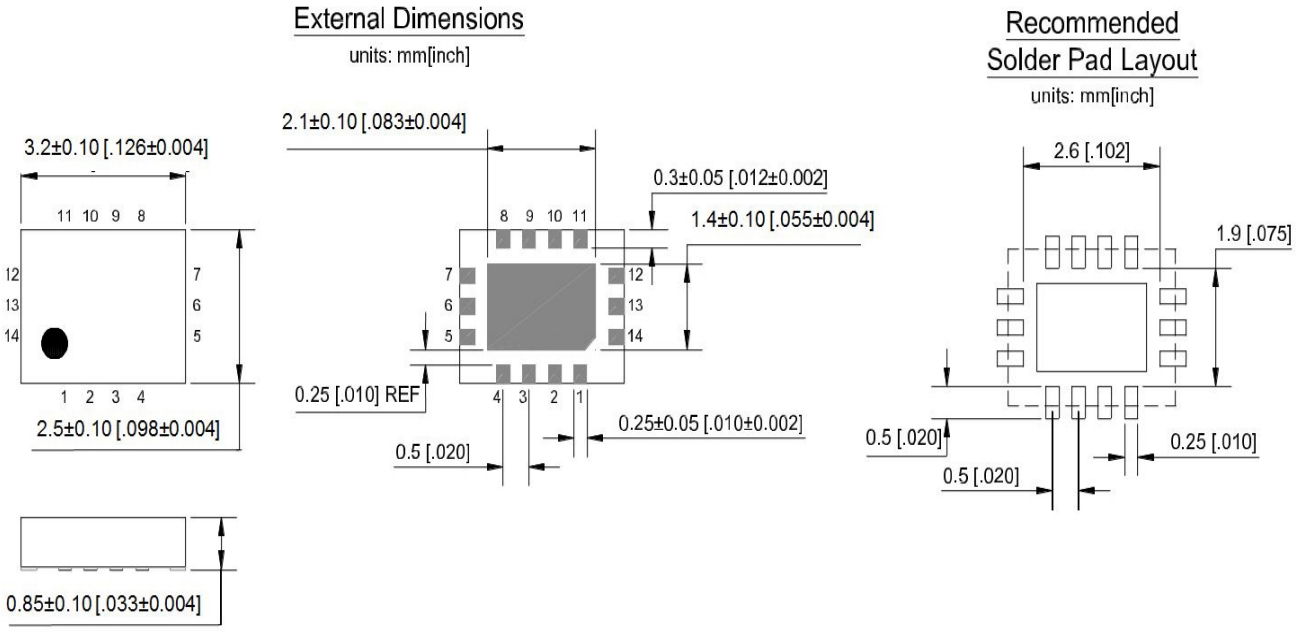


Figure 5. Solder Reflow Profile

Package Information[7]



3.2mm x 2.5mm 14 Lead Plastic Package

Notes:

6. Connect the exposed die paddle to ground.
7. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.