Description

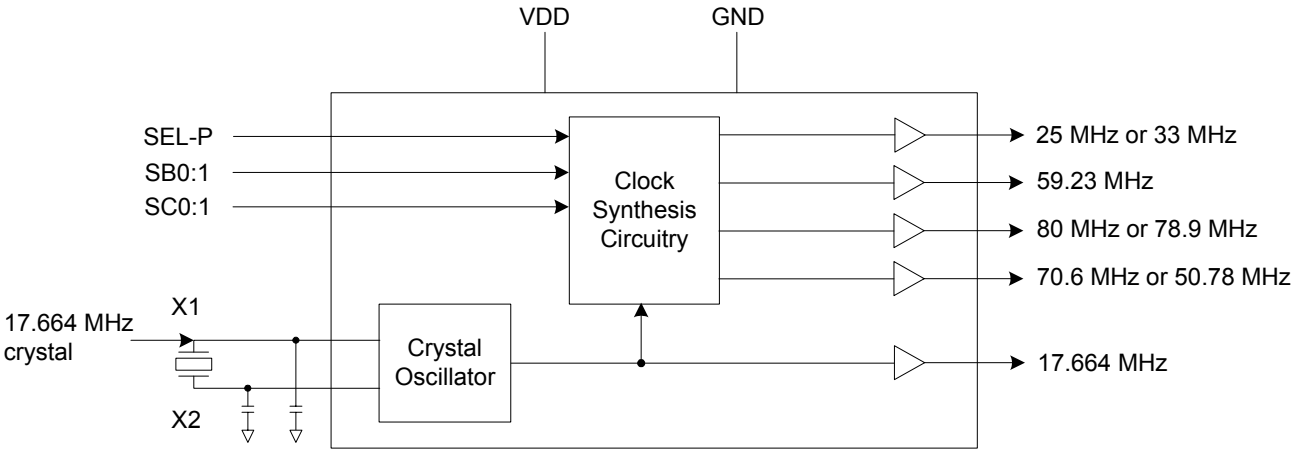
The ICS650-11C is a low-cost, low-jitter, high-performance clock synthesizer optimized for Alcatel system requirements. Using analog/digital Phase-Locked Loop (PLL) techniques, the device accepts a parallel resonant 17.664 MHz crystal input to produce up to five output clocks.

Features

- Packaged in 20-pin tiny SSOP (QSOP)
- Operating VDD of 3.3 V
- Inexpensive 17.664 MHz crystal or clock input
- Provides selectable 80 MHz or 78.9 MHz clock
- Provides selectable 59.23 MHz clock
- Provides selectable 25 MHz or 33 MHz clock
- Provides selectable 70.6 MHz or 50.78 MHz clock
- Provides fixed 17.664 MHz clock
- Duty cycle of 40/60
- Advanced, low-power CMOS process
- Industrial temperature range

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



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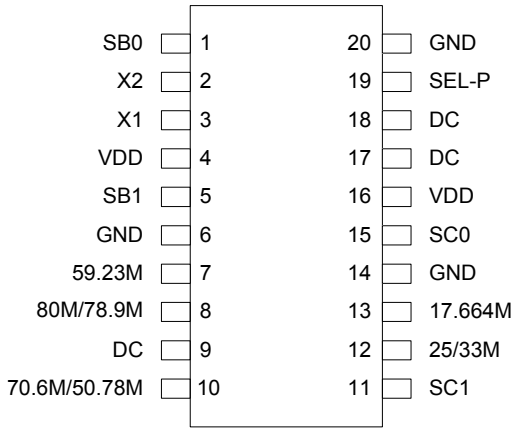
Pin Assignment



20-pin (150 mil) SSOP

Processor Clock (MHz)

SEL-P	Pin 12
0	33.0
1	25.0

0 = connect directly to ground
1 = connect directly to VDD

SC Clock (MHz)

SC1	SC0	Pin 10
0	0	OFF
0	1	70.656
1	0	50.784

SB Clock (MHz)

SB1	SB0	Pin 7	Pin 8
0	0	Low	80
1	1	59.23	78.9

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	SB0	Input	Input pin. See table above.
2	X2	XO	Crystal connection. Connect to a parallel mode 17.664 MHz crystal. Leave open for clock.
3	X1	XI	Crystal connection. Connect to a parallel mode 17.664 MHz crystal or clock.
4, 16	VDD	Power	Connect to VDD. Must be same value as other VDD's. Decouple with pin 6.
5	SB1	Input	Select pin. See table above.
6, 14, 20	GND	Power	Connect to ground.
7	59.32M	Output	B1 clock. See table above.
8	80M/78.9M	Output	B2 clock. See table above.
9, 17, 18	DC	—	Don't connect. Do not connect this pin to anything.
10	70.6M/50.78M	Output	SC clock. See table above.
11	SC1	Input	Select pin. See table above.
12	25/33M	Output	25 MHz or 33 MHz clock output. Determined by SEL-P per table above.
13	17.664M	Output	17.664 MHz buffered reference clock output.
15	SC0	Input	Select pin. See table above.
19	SEL-P	Input	Select pin. Determines frequency of pin 12 per table above.

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External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS650-11C must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS650-11C. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

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Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-11C. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Conditions	Rating
Supply Voltage, VDD	Referenced to GND	7 V
All Inputs and Outputs	Referenced to GND	-0.5 V to VDD+0.5 V
Ambient Operating Temperature		-40 to +85° C
Storage Temperature		-65 to +150° C
Soldering Temperature	Max. of 10 seconds	260° C

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0	3.3	3.6	V
Input High Voltage	V_{IH}	SEL input	VDD-0.5			V
Input Low Voltage	V_{IL}	SEL input			0.5	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Operating Supply Current	I_{DD}	No Load, Note 1		25		mA
Short Circuit Current	I_{OS}	Each output		±50		mA
Input Capacitance		Except X1, X2		7		pF

Notes:

1. With all clocks at highest frequencies.

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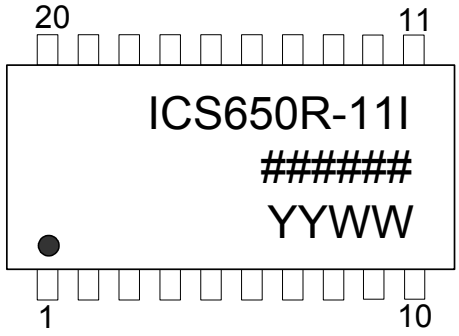
AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Crystal or Clock Frequency				17.664		MHz
Output Clocks Accuracy (synthesis error)		25 MHz		0	-0.05	%
		33 MHz			0.04	%
		80 MHz			-0.04	%
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V			1.5	ns
Output Clock Fall Time	t_{OF}	2.0 to 0.8 V			1.5	ns
Output Clock Duty Cycle		80 MHz, at VDD/2	40	50	60	%
		Other clocks, at VDD/2	45	50	55	%
Cycle-to-cycle Jitter		25/33 MHz, 80 MHz		295		ps

Marking Diagram



Notes:

1. ###### is the lot number.

2. YYWW is the last two digits of the year and the week number the part was assembled.

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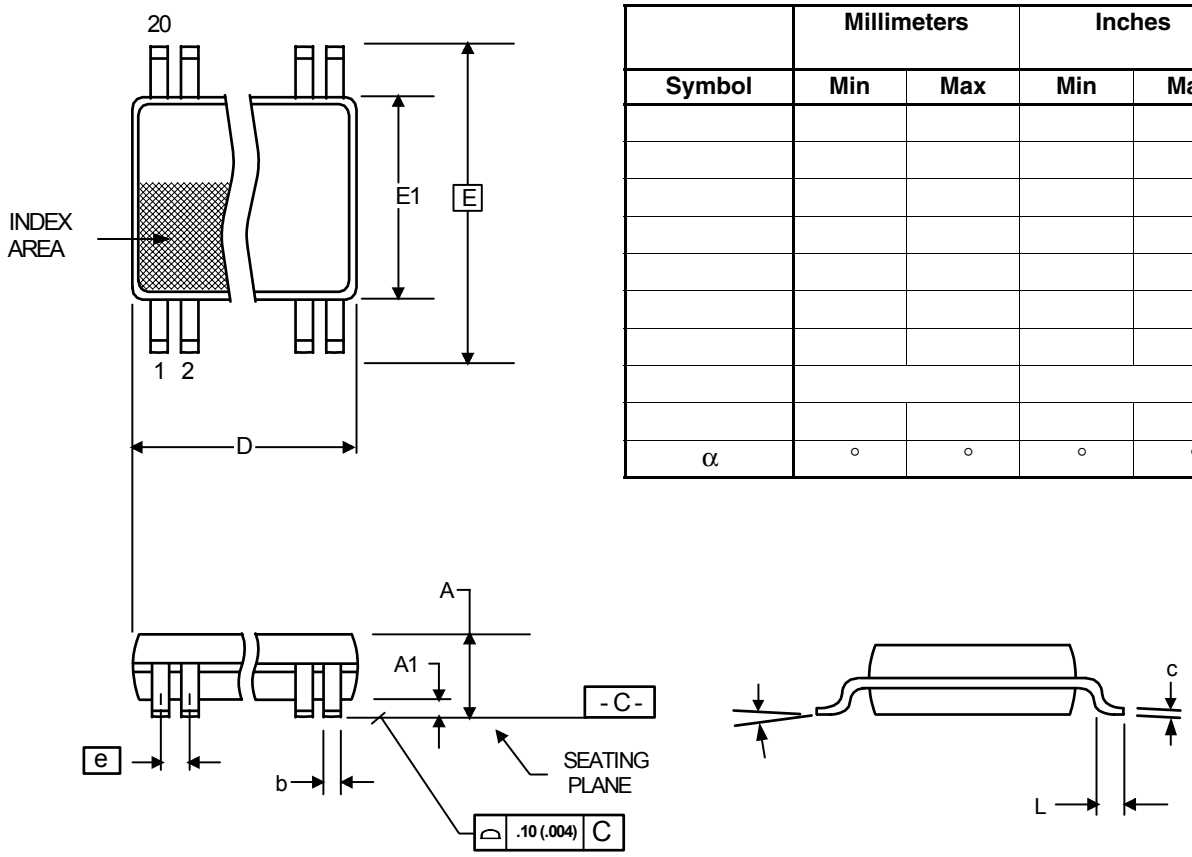
Package Outline and Package Dimensions (20-pin SSOP)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
α	°	°	°	°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650R-11I	ICS650R-11I	Tubes	20-pin SSOP	-40 to +85° C
650R-11IT	ICS650R-11I	Tape and Reel	20-pin SSOP	-40 to +85° C

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