Test Results of the HTADC12 12 Bit Analog to Digital Converter at 250°C

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Abstract

This paper discusses the results of leveraging advances in high temperature electronics and integrating them for new applications and improved system performance. It centers on the development of the 250°C High Temperature (HT) SOI CMOS process technology and its application to an Analog To Digital Converter (ADC) Integrated Circuit (IC). Honeywell has completed the development of a 12 bit Successive Approximation ADC operating at 100kS/s for sensor data processing and control applications in extreme environments ranging from -55°C to 250°C.

1. Introduction

Due to the need for High Temperature (HT) electronics, small size and ability to survive in very rugged environments including conversion of analog sensor data to digital data for processing, the performance results of a new high temperature Analog to Digital Converter (ADC) is being presented. Starting from a base high temperature SOI CMOS technology, key mixed signal functions are developed and then integrated. The HTADC12 is designed and manufactured for long life at high temperatures (250°C) and high reliability in extremely harsh environments.

2. Technology Development and Application

The 12-bit ADC applies new technology and techniques derived from the high-temperature wafer process and design platforms developed under the U.S. Dept. of Energy DeepTrek program. It is a key component for high temperature conversion of analog sensor and control signals to digital data to create smart sensors.

3. HT SOI CMOS Technology

The Integrated Circuits (ICs) are manufactured on 0.8um Silicon On Insulator (SOI) CMOS technology operating at 5 volts. SOI CMOS has a number of features which allow for electronics to operate at temperatures at and above 250°C.

- Lower Leakage Current – The full oxide isolation SOI technology minimizes junction size and the leakage current which doubles every 10°C (above ≈170°C). The design of the transistors also re-targets transistor threshold voltage implants to reduce leakage.

- Lifetime Extension at High Temp – Electromigration increases at high temperatures and so the IC design and layout rules lower the current densities, increasing reliability and lifetime.

4. Typical Specifications

Parameter	Value
Supply Voltage	5V
Internal ADC Clock	4 MHz
Sampling Rate	100 kS/s
Operating Current	2 mA @ 25°C 3 mA @ 225°C
Power Consumption	10 mW @ 25°C 15mW @ 225°C

5. Process, Design and Architecture Features

In order to deliver the performance over the wide temperature range, a number of special techniques are implemented at various stages of development. Some specific elements of the development include:

- Transistor modeling for highly linear analog requirements
- Minimize leakage through transistor balancing
- Balanced circuit design to temperature compensate the performance
- Wafer Level Trimming
- Flexible digital interface: format and speed

6. HTADC12 Description

The HTADC12 is a high temperature, single supply, 12-bit, 100kS/s, analog-to-digital converter with on-chip buffered voltage reference and an on-chip auxiliary buffer op amp. The HTADC12 uses a Successive Approximation Register (SAR) architecture that does not require an input sample-and-hold amplifier to provide 12-bit accuracy at 100 kS/s data rates, and no missing codes over the full operating temperature range of -55^{O}C to +250^{O}C.

The input of the HTADC12 allows for easy interfacing to sensors and op amps like the HTOP01 for data conversion applications. The direct input supports 0V to 2.5V signals and IC also includes an on-chip buffer amp to allow for full 5V input signals. The digital output has both a serial and parallel digital interface configuration.

Data conversions are triggered with a simple logic input signal and are clocked with an internal 4MHz clock.

Voltage Reference

The 12-bit ADC has an internal voltage reference of 2.49V to 2.51V over all conditions (-55^{O}C to +250^{O}C). This reference is also buffered and provided as an output. An external reference may also be used.

Data Output Formats

There are three output formats: 12 bit parallel, two 8 bit parallel, and serial.

The parallel data can be presented as either 12 straight binary bits or configured for a "two-byte READ" for use with 8 bit processor busses.

12-Bit Data Readout in 8-Bit Systems: The HTADC12's 12-bit parallel data output can be read out by an 8-bit system in two 8-bit bytes. In this mode, the 8 MSB bit positions of the 12-bit output are utilized as the 8-bit bus.

Address control of the byte of interest is handled by the logic state of the A0 control line.

- When A0=0, the output data assumes its normal 12-bit format with bits D11-D4 of the 12-bit word forming the 1st data byte.
- When A0=1, bits D3-D0 followed by 4 logic zeroes are superimposed onto the 8 MSB bit positions, forming the 2nd data byte.

Data Output Pins	Data Output Values	
	AO = 0 (READ bits D4 – D11)	AO = 1 (READ bits D0 – D3)
D11	D11	**D3**
D10	D10	**D2**
D9	D9	**D1**
D8	D8	**D0**
D7	D7	"0"
D6	D6	"0"
D5	D5	"0"
D4	D4	"0"
D3	D3	D3
D2	D2	D2
D1	D1	D1
D0	D0	D0

8 Bit Bus

Serial Output Control

The data can also be read out serially on the SDO pin. The data is valid just prior to the STS signal and is clocked out with the SCLK falling edge with MSB first.

High Temp and Ruggedized Package

The HTADC12 is packaged in a 14 or 28 lead ceramic DIP package with serial and parallel outputs, respectively.

7. Electrical Performance Characteristics

Symbol	Parameter	Conditions(1)	Limits			Units
			Min	Typ	Max	
# of Bits	Resolution			12		Bits
INL	Integral Non-Linearity		-2		+2	LSB
DNL	Differential Non-Linearity		-0.5		+0.5	LSB
Offset	Offset Error	VIN value @ VOUT = .5 LSB	-3	0	+3	LSB
FS_ERR	Full Scale Calibration Error	VREFIN = 2.5V, T=25°C			0.3	% of FS
Δ VRO	VREFOUT (Initial Error)	T = 25°C (delta from 2.5V)	-10		+10	mV
Δ VRO-TEMP	VREFOUT Drift with temp	VDD = 5.0V	-20		+20	mV
VRN	VREFOUT Noise	f = 0.1Hz to 10 Hz		110		µV rms
TCONV	Conversion Time		9		11	µs
FSCLK	Serial Clock Frequency	C_{load} = 10pF			40	MHz
Δ R/R	Aux Amp Input Resistor Divider (/2)Matching		-0.1		+0.1	%

(1) Unless otherwise specified, specifications apply over the full VDD-VSS range from -55°C to 250°C, VDDA externally connected to VDD, VSSA externally connected to VSS.

8. HTADC12 Test Results

Test Environments

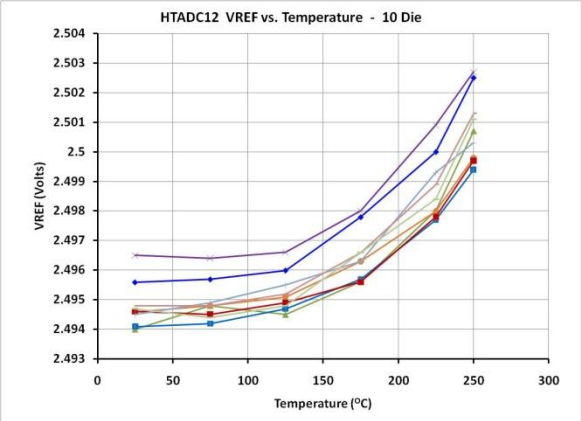
The test results shown are derived from two different wafer test environments. These include a lab test setup which is capable of reaching 275^{O}C and the automated Manufacturing wafer test setup and program capable of testing at 200^{O}C. The Manufacturing wafer test provides more accurate measurements.

It should additionally be noted that all test results presented here are based on wafer probe data, which is not the optimum test environment for making precision measurements. This is particularly true for INL and DNL. Packaged parts will need to be evaluated on a dedicated test board to demonstrate ultimate performance capability.

Internal Voltage Reference

The HTADC12 has it's own internal reference voltage of 2.49V to 2.51V over all conditions (-55^{O}C to +250^{O}C). Depending on the configuration of the ADC, the VREF voltage is used both internally and externally

VREF is designed to be laser trimmed for optimal performance over silicon process and temperature. The typical voltage drift with temperature is 5mV to 7mV. A plot of VREF (after trimming), taken at the wafer level of several devices, is shown below.

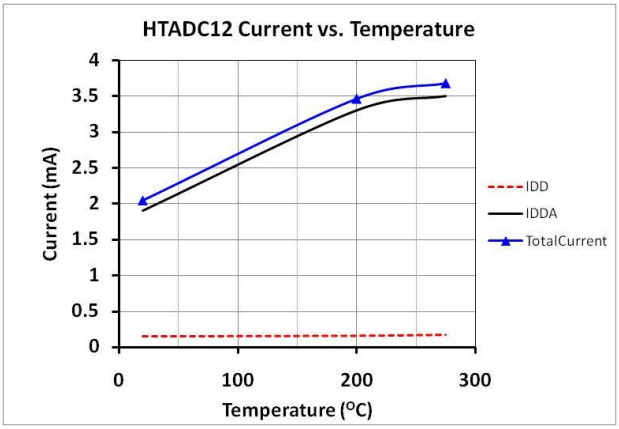


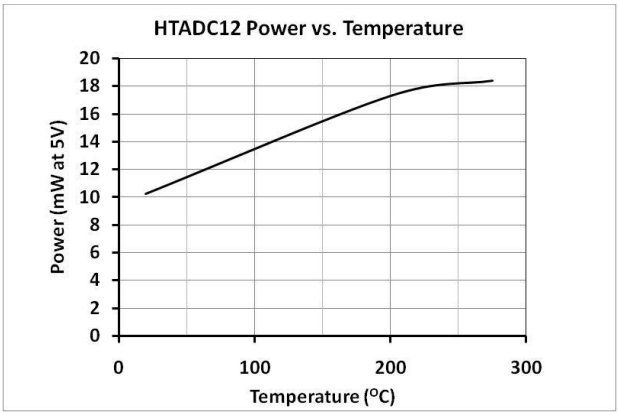
Buffer Amplifier Resistors Matching

A key component of the auxiliary buffer amplifier is the on-chip resistors. These resistors must be accurate and maintain their value over the wide temperature range. High quality, wide temperature range resistors combined with a high performance op amp allows for enhanced additional scaling and filtering capability while minimizing the board area required. The specification for the resistor mismatch is 0.1%. Measurements of eight devices yielded a worst case performance of 0.056% at room temperature and 0.060% at 275^{o}C. This illustrates the high stability of the resistors over temperature.

Current And Power Consumption

The HTADC12 has two power supplies, VDD and VDDA (analog). The analog circuitry draws current that is approximately Proportional To Absolute Temperature (PTAT). The digital supply is relatively independent of temperature. Measurements were made on both the lab and Production testers. When not in use, the device can be put in a low power mode (NAP), in which the current is reduced to ~0.8 mA.





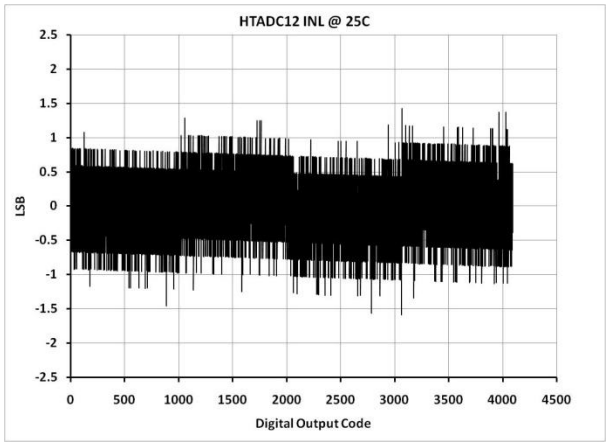
Integral Non-Linearity

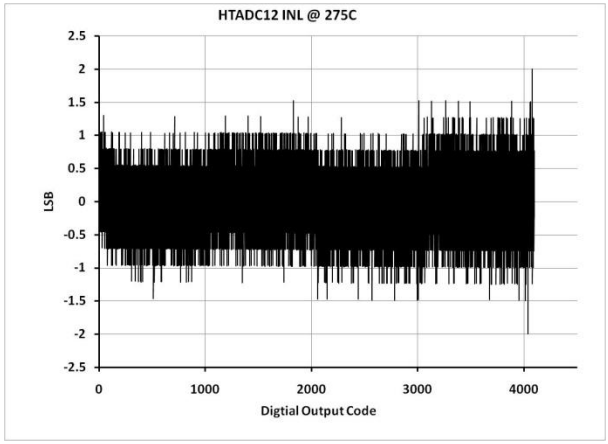
INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line. The INL-error magnitude then depends directly on the position chosen for this straight line. The INL specification is measured after both static offset and gain errors have been nullified, and can be described as follows:

INL = | [(VD - VZERO)/VLSB-IDEAL] - D | , where 0 < D < 2N-1.

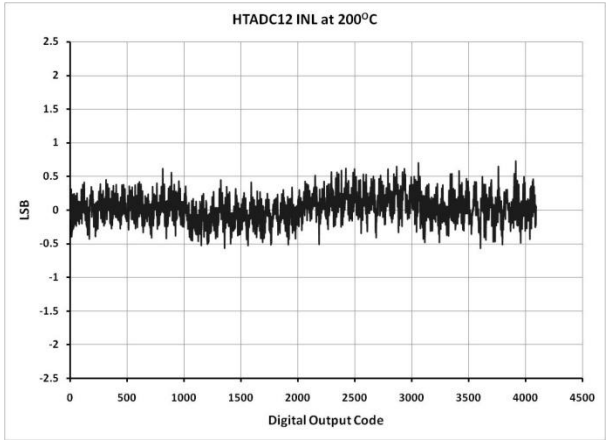
VD is the analog value represented by the digital output code D, N is the ADC's resolution, VZERO is the minimum analog input corresponding to an all-zero output code, and VLSB-IDEAL is the ideal spacing for two adjacent output codes.

Lab Measurements – INL at 25°C and 275°C





Manufacturing Test – INL at 200°C



Differential Non-Linearity

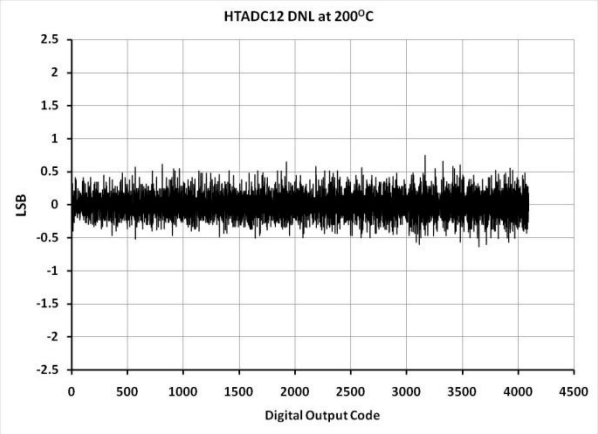
A DNL error specification of less than or equal to 1LSB guarantees a monotonic transfer function with no missing codes.

DNL is specified after the static gain error has been removed. It is defined as follows:

DNL = |[(VD+1- VD)/VLSB-IDEAL - 1] | , where 0 < D < 2N - 2.

VD is the physical value corresponding to the digital output code D, N is the ADC resolution, and VLSB-IDEAL is the ideal spacing for two adjacent digital codes.

Manufacturing Test – DNL at 200^{O}C



Summary and Conclusions

In order to fulfill the need for higher performance sensor and analog data conversion at extreme temperatures, the test results for the 12 bit ADC have shown stable, predictable performance over a temperature range of -55^{O}C to +250^{O}C. Leveraging advances in high temperature SOI CMOS, circuit design and manufacturing techniques, a low power ADC with many features for "ease of use" has been developed and manufactured.

9. References

(1) Honeywell "*HTADC12*" Datasheet, dated April 2009

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