PIC16(L)F19195/6/7

PIC16(L)F19195/6/7 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F19195/6/7 family devices that you have received conform functionally to the current Device Data Sheet (DS40001873**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F19195/6/7 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F19195/6/7 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A1	A3
PIC16F19195	3084h	2001h	2003h
PIC16LF19195	3086h	2001h	2003h
PIC16F19196	3085h	2001h	2003h
PIC16LF19196	3087h	2001h	2003h
PIC16F19197	30A2h	2001h	2003h
PIC16LF19197	30A3h	2001h	2003h

Note 1: The Device and Revision IDs is located at the respective addresses 8006h and 8005h of configuration memory space.

2: Refer to the *"PIC16(L)F1919X Memory Programming Specification"* (DS40001846) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Summary	Affected Revisions	
				A1	A3
Analog-to-Digital Converter with Computation (ADC^2)	ADC^2 Clock Selection	1.1	Static MSB with FRC selected as ADC clock source.	X	
	ADC^2 with Fixed Voltage Reference (FVR)	1.2	Using the FVR as the ADC positive voltage reference can cause missing codes.	X	
Reset and VBAT	VBAT with ULPBOR	2.1	Higher current with ULPBOR active.	X	
Liquid Crystal Display (LCD) Controller	LP Ladder	3.1	Resistance of LP ladder is different than what is indicated in the data sheet.	X	
	Internal VLCD3 Measurement	3.2	Non stable readings.	X	
	LCD Charge Pump Low-Power mode	3.3	The LCD Charge Pump Low-Power (Low-Current (LC)) mode is calibrated but not tested.	X	
	1/2 MUX, 1/2 Bias with External Resistor Ladder	3.4	1/2 MUX, 1/2 Bias with External Resistor Ladder is not operational.	X	
Windowed Watchdog Timer (WWDT)	Watchdog Timer Clock Source	4.1	WWDT only operates from the LFINTOSC clock source.	X	
Comparator (CMP)	C2 Low-Power Clocked Comparator	5.1	Unstable output.	X	X
Electrical Specifications	VBAT current specification.	6.1	Higher typical current.	X	
	SMBus VIL Level	6.2	The maximum VIL level changes when VDD is below 4.0V.	X	X
	Program Flash Memory (PFM) Endurance	6.3	The PFM endurance is lower than specified.	X	
	Internal Oscillator Frequency Accuracy	6.4	Internal oscillator frequency accuracy may be higher than specified at temperatures between 0 and 60°C.	X	X
	Fixed Voltage Reference (FVR) Accuracy	6.5	Fixed Voltage Reference (FVR) output tolerance may be higher than specified at temperatures below -20°C.	X	
	Nonvolatile Memory (NVM) for LF Devices	6.6	Performing a row erase through the NVMREG access may not execute as expected when VDD is lowered from >3.3V down to <2.0V between +25°C and -40°C.	X	X
	Min. VDD Specification	6.7	VDDMIN specifications are changed for LF devices only.	X	X

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Analog-to-Digital Converter with Computation (ADC^2)

1.1 ADC^2 Clock Selection

The ADC does not function properly if FRC is selected as its clock source resulting in the MSB being stuck as a '0' or a '1'. This also prohibits using the ADC module in Sleep mode.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

1.2 ADC^2 with Fixed Voltage Reference (FVR)

Using the FVR as the positive voltage reference (V_{REF+}) for the ADC, can cause an increase in missing codes.

Work around

Method 1: Increase the bit conversion time, known as TAD, to 8 µs or higher.

Method 2: Use V_{DD} as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1	A3						
X							

2. Module: Reset and V_{BAT}

2.1 V_{BAT} with ULPBOR

In order to avoid high I_{BAT} currents of 10 µA or greater, when utilizing V_{BAT} to provide battery back-up the ULPBOR should not be activated. When the part is used in this fashion, V_{DD} should also be either off (0 volts) or >1.5V.

Work around

Do not use V_{BAT} along with ULPBOR.

Affected Silicon Revisions

A1	A3						
X							

3. Module: Liquid Crystal Display (LCD) Controller

3.1 LP Ladder

The resistance of the LP Resistor Ladder is 6.6 M-ohms rather than the 3.3 M-ohms indicated in the data sheet.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

3.2 Internal VLCD3 Measurement

The ¼ scale tap point provided on the LP Resistor Ladder for use together with the ADC does not provide stable readings to support monitoring of the LCD pump output level.

Work around

Measure the VLCD3 via an external ADC.

Affected Silicon Revisions

A1	A3						
X							

3.3 LCD Charge Pump Low-Power Mode

The LCD Charge Pump Low-Power (Low Current (LC)) mode is calibrated to a nominal value but not tested.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

3.4 1/2 MUX, 1/2 Bias with External Resistor Ladder

The 1/2 MUX, 1/2 bias with external resistor ladder mode of operation is non-functional.

Work around

For 1/2 MUX, 1/2 Bias mode operation use the internal LP, MP or HP ladder.

Affected Silicon Revisions

A1	A3						
X							

4. Module: Windowed Watchdog Timer (WWDT)

4.1 Watchdog Timer Clock Source

When the WDTCS <2:0> bits of the WDTCON1 register are set to either the MFINTOSC (b'001') or the SOSC ('b010') clock source, the WWDT does not operate.

Work around

Use the LFINTOSC (b'000') as the clock source for the WWDT.

Affected Silicon Revisions

A1	A3						
X							

5. Module: Comparator (CMP)

5.1 C2 Low-Power Clocked Comparator

The output of the Low-Power Clocked Comparator (CMP2) is unstable and is not recommended for use.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

6. Module: Electrical Specifications

6.1. V_{BAT} Current Specification

I_{BAT} with V_{BAT}, SOSC and RTCC active ($V_{BAT} > V_{DD}$) is higher than the 400 nA typical target shown on the data sheet. The typical current observed on rev A1 parts at 25°C will be 1.3 µA at 3.0V V_{DD}.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

6.2 SMBus V_{IL} Level

When the V_{DD} voltage level supplied to the device is 4.0V and above, the maximum SMBus voltage level for the V_{IL} parameter is 0.8V. When V_{DD} drops below 4.0V, the maximum SMBus voltage level for V_{IL} drops to 0.7V.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

6.3 Program Flash Memory Endurance

The minimum value for the Program Flash Memory (PFM) endurance specification, called out as parameter number MEM30 in the data sheet, is 1K cycles.

Work around

None.

Affected Silicon Revisions

A1	A3						
X							

6.4 Internal Oscillator Frequency Accuracy

HFINTOSC frequency accuracy is greater than shown on the data sheet in Figure 39-6 and listed in Note 1 of the same figure. Over the temperature range of 0 to 60°C, and over V_{DD} range of 2.3V to 5.5V, the internal oscillator frequency accuracy has changed from +/-2% to +/-3%.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

6.5 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A1	A3						
X							

6.6 Nonvolatile Memory (NVM) for LF Devices

Performing a row erase through the NVMREG access on LF device may not execute as expected when V_{DD} is lowered from >3.3V down to <2.0V before or during the row erase while also operating between +25°C and -40°C.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

6.7 Min V_{DD} Specification

V_{DDMIN} specifications are changed for LF devices only.

V_{DDMIN} at -40°C to 0°C = 2.3V.

V_{DDMIN} at 0°C to 25°C = 2.1V.

Work around

None.

Affected Silicon Revisions

A1	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001873**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Analog-to-Digital Converter with Computations (ADC^2)

Table 19-1 cells should be shaded if they are outside of the recommended TAD parameter range. TAD values that are outside of the recommended range for this device are shaded. The corrected table is as follows:

TABLE 19-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES(1,4)

ADC Clock Period (TAD)		Device Frequency (FOSC)					
ADC Clock Source	**CS<5:0>**	**32 MHz**	**20 MHz**	**16 MHz**	**8 MHz**	**4 MHz**	**1 MHz**
FOSC/2	000000	62.5 ns(2)	100 ns(2)	125 ns(2)	250 ns(2)	**500 ns**	2.0 µs
FOSC/4	000001	125 ns(2)	200 ns(2)	250 ns(2)	**500 ns**	1.0 µs	4.0 µs
FOSC/6	000010	187.5 ns(2)	300 ns(2)	375 ns(2)	**750 ns**	1.5 µs	6.0 µs
FOSC/8	000011	250 ns(2)	400 ns(2)	**500 ns**	1.0 µs	2.0 µs	8.0 µs
...	...	...	...	...	...	...	...
FOSC/16	000111	**500 ns**	**800 ns**	1.0 µs	2.0 µs	4.0 µs	16.0 µs(3)
...	...	...	...	...	...	...	...
FOSC/128	111111	4.0 µs	6.4 µs	8.0 µs	16.0 µs(3)	32.0 µs(2)	128.0 µs(2)
FRC	CS(ADCON0<4>) = 1	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs	1.0-6.0 µs

Legend: Shaded cells are outside of recommended range.

Note 1: See TAD parameter for FRC source typical TAD value.

2: These values violate the required TAD time.

3: Outside the recommended TAD time.

4: The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock FOSC. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

2. Module: Real Time Clock and Calendar (RTCC)

A new note is added to section **24.1.2 Write Lock**, with the following text:

The RTCEN bit of the RTCCON register is synchronized to the SOSC and will not be set until the external oscillator is available. The first time that the RTCEN bit is set, there could be a delay between when the bit is set in software and when the bit is set in the RTCCON register, if an external crystal is used as the clock source.

This potential delay is based upon the start-up time of the crystal, as the RTCEN bit of the RTCCON register will not set until the external oscillator is stable and ready. The start-up time of the specific external crystal must be considered when initializing the RTCC module to ensure that the RTCC module is enabled before the RTCWREN bit is cleared. It is recommended that the RTCEN bit is polled after setting it to ensure that it is set before clearing the RTCWREN bit.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (03/2017)

Initial release of this document; issued for revision A1. Includes silicon issues 1.1 (ADC^2), 1.2 (ADC^2), 2.1 (V_{BAT}), 3.1 (LCD), 3.2 (LCD), 3.3 (LCD), 3.4 (LCD), 4.1 (WWDT), 5.1 (CMP),

Electrical Specifications: 6.1 ADC, 6.2 V_{BAT}, 6.3 SMBus, 6.4 Program Flash Memory, and 6.5 FVR.

Data Sheet Clarifications:

Module 1: LCD

Rev B Document (10/2017)

Removed Module 6.1: ADC Offset and Gain Error; Added Module 6.4: Internal Oscillator Frequency Accuracy; Added Module 6.6: Nonvolatile Memory (NVM) for LF Devices; Added affected revision A3; Other minor corrections.

Data Sheet Clarifications: Removed Module 1 (Data Sheet updated).

Rev C Document (01/2018)

Added Module 6.7: Min. V_{DD} Specifications. Updated Modules 6.3, 6.4, and 6.5 “Affected Silicon Revisions” Tables.

Rev D Document (05/2018)

Data Sheet Clarifications: Added Module 1: Analog-to-Digital with Computation (ADC^2) and Module 2: Real Time Clock and Calendar (RTCC).

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