LX23224

4 Channel EDGE Lit LED Display Driver with 1 DC/DC PSU Controller

PRODUCTION DATASHEET

Introduction

DESCRIPTION

The LX23224 is a four channel LED driver for LED backlight applications in LCD TVs and monitors. It integrates a DC/DC block with peak current mode control and four PWM controllers to drive four LED strings. The DC/DC control loop adjusts the boost voltage for maximum power efficiency.

LED string short circuit or open circuit conditions are detected, flagged, and protected against.

Internal linear regulators provide 12V and 5V rails to drive internal circuitry from V_{IN} voltage. Alternatively a 12V supply can be fed directly to the device.

DC/DC switching frequency can be synchronized between multiple devices to prevent beat frequency interference.

LX23224 supports Direct Digital PWM LED dimming.

LX23224 is provided in 36 pin SSOP and 36 pin QFN packages.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

KEY FEATURES

- EDGE-Lit LED Backlight Driver for LCD TVs and Monitor Displays
- Direct Digital PWM LED Dimming Operation
- Supports LED PWM Dimming Frequency up to 2kHz
- 2% Precision Current Control of Four LED Strings (string to string)
- 3% Precision Current Control (chip to chip)
- Supports Four LED Strings with Control and Protection
- LED String Currents are Completely User Programmable
- 100kHz to 300kHz Constant Switching Frequency Power Conversion
- Supports DC/DC Synchronization Across Multiple ICs
- Open String and Over-Temperature Protection and Indication
- LED String Short Circuit Protection and Indication
- RoHS compliant

PACKAGE ORDER INFO		THERMAL DATA
T_A (°C) -40 to +85	LX23224IDB (Tube) LX23224IDB-TR (Tape and Reel)	θ_{JA} = 70°C/W 36 SSOP leaded package According to JESD51-7
	LX23224ILQ (Tube) LX23224ILQ-TR (Tape and Reel)	θ_{JA} = 32°C/W 36 QFN package According to JESD51-7

- RoHS Compliant / Pb-free

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} levels are guidelines for the thermal performance of the device/pc-board system. All of the above assumes no ambient airflow.

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

PACKAGE PIN OUT

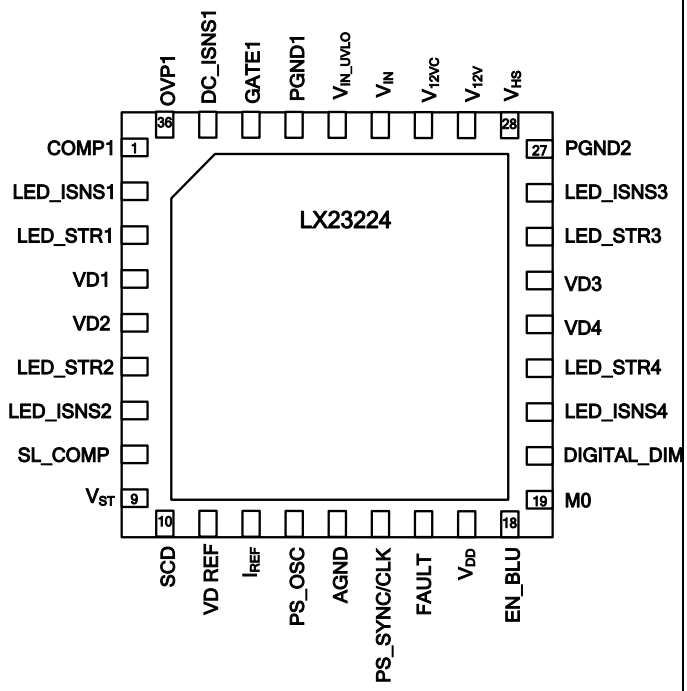


Figure 1: LX23224ILQ QFN Package Pin Out

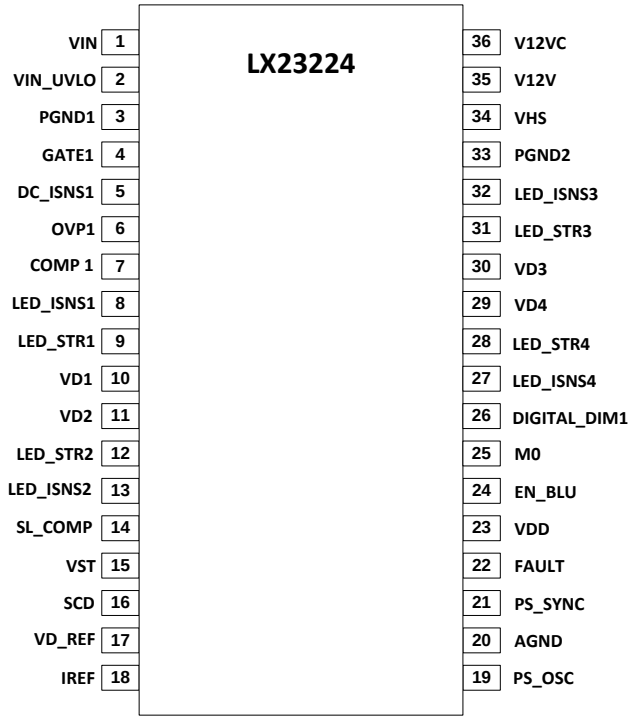


Figure 2: LX23224IDB SSOP Package Pin Out

ABSOLUTE MAXIMUM RATINGS

V_{IN} Supply Input Voltage ..... -0.3V to 45V
V_{12V} Supply Input Voltage ..... -0.3V to 15V
V_{12VC} ..... V_{12V} -0.3V to V_{12V} +2V
V_{IO} Input Voltage ..... -0.3V to V_{DD}+0.3V
Gate1, LED_STR1-LED_STR 4, VD1-VD4 ..... -0.3V to V_{12V} +0.3V
FAULT,LED ISNS 1-LED ISNS4 ..... -0.3V to +6V
Between any two grounds. ..... -0.3V to+ 0.3V
Operating Ambient Temperature Range ..... -40 to 85°C
Maximum Operating Junction Temperature ..... 150°C
HBM ESD Protection at all I/O pins ..... +/- 2.5 kV
CDM ESD Protection at all I/O pins ..... +/- 1.5kV
MM ESD Protection at all I/O pins ..... +/- 250V
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering 10 seconds) ..... 300°C
Package Peak Temperature for Solder Reflow (40 seconds maximum exposure) ..... 260°C (+0, -5°C)

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

RECOMMENDED OPERATING CONDITIONS

V_{IN} Supply Input Voltage ..... 15 to 30V
V_{12V} Supply Input Voltage when driven from an external supply ..... 10 to 15V
Operating Ambient Temperature Range ..... -40 to 85°C
Minimum PWM pulse width 20µS
R_{IREF} 30.1kΩ

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

Electrical Specifications

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply for operating ambient temperature -10°C ≤ Tamb ≤ +85°C.

IC Supply Specifications

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX23224 MIN	LX23224 TYP	LX23224 MAX	UNIT
IC Supply (VIN = 24V, Boost switches at 300kHz, V_{12VC} pin is shorted to V_{12V} pin)						
Supply Voltage	V_{IN}	Input condition when V_{IN} drives the 12V internal linear regulator	15	24	40	V
Input Supply Current	I_{IN}	V_{IN} = 24V, LED PWM 50% duty at 2kHz, DC/DC switching at 300kHz, gate drivers loaded by 1000pF		23	30	mA
		LED dimming at 0%		5	8	
Sleep Current	I_{SLEEP}	EN_BLU = Logic low, V_{DD} and V_{12V} are active and available to drive external circuitry.		3	5	mA
References and Supply Voltages (I_{REF}, V_{12VC}, V_{12V}, V_{DD}, V_{HS})						
I_{REF} Output voltage	V_{IREF}	Loaded with a 30.1kΩ resistor	1.181	1.201	1.222	V
12 V_{DC} Input Voltage	V_{12V}	Input condition when using an external 12V supply to drive V_{12V}	10	12	15	V
12V Regulated Voltage Output	V_{12V}	15V ≤ V_{IN} ≤ 30V, 0 ≤ I ≤50mA Pins V_{12V} and V_{12VC} are connected together	10.8	12	13.2	V
5V Regulated Voltage Output	V_{DD}	10V≤V_{12V}≤15V, 0 ≤ I≤10 mA	4.75	5	5.25	V
V_{12VC} Output Current	I_{12VC}	V_{12VC} pin is shorted to V_{12V} pin. Available for external use	2			mA
V_{DD} Output Current	I_{VDD}	Available for external use	1			mA

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX23224 MIN	LX23224 TYP	LX23224 MAX	UNIT
LED Current Accuracy (20 mA < ILED < 350 mA @ 100% duty cycle, VSENSE = 350 mV)						
LED Current Accuracy Chip to Chip		-10°C ≤T_{amb} ≤ +85°C			±3	%
		+50° C ≤T_{amb} ≤+70°C			±2	%
LED Current Matching (20 mA < ILED < 350 mA @ 100% duty cycle, VSENSE = 350 mV)						
LED Current Matching String to String		-10°C ≤T_{amb} ≤ +85°C			±2	%
		+50° C ≤T_{amb} ≤+70°C			±1	%
LED NFET Driver (LED_ISNS1-4,LED_STR1-4)						
LED Current Sense Accuracy	V_{SENSE}	LED_ISNS voltage absolute accuracy	340	348	355	mV
Gate Drive Range	V_{GD_LED}		0		V_{12V}	V
DC/DC oscillator (PS_SYNC/CLK)						
PS reference voltage	V_{PS}	Loaded with a 30.1kΩ resistor.	1.127	1.154	1.173	V
Upper oscillator frequency	f_{OSC_UPPER}	R_{PS_OSC} = 30.1kΩ DC/DC switching frequency is 1/2 of the oscillator frequency	0.54	0.6	0.66	MHz
Lower oscillator frequency	f_{OSC_LOWER}	R_{PS_OSC} = 90.9kΩ DC/DC switching frequency is 1/2 of the oscillator frequency	0.18	0.20	0.22	MHz
DC/DC NFET Driver (GATE1)						
DC/DC Maximum Duty Cycle	DC_{MAX}			90		%
Pull up Resistance				9	18	Ω
Pull down Resistance				6	12	Ω
DC/DC Current Sense section (DC_ISNS1)						
Maximum Sense Input Voltage	V_{SENSE}		180	200	220	mV
Leading Edge Blanking	t_{BLANK}		75	100	125	ns
Drain Voltage Sensing section (VD1, VD2, VD3, VD4)						
VDMIN Accuracy		WRT VD_REF	-0.1	0	.1	V
VD bias Current		Bias for external blocking diode		90		µA
LED short circuit detection level (SCD, VD1, VD2, VD3, VD4)						
Differential SCD threshold	V_{SCD}	Difference between VDmax and Vdmin, R_{SCD} = 100kΩ,	7.6	8	8.4	V
Absolute SCD threshold		Measured WRT V12V		92		%
SCD bias current				0.6/R_{IREF}		A
V_{DMIN} Reference (VD_REF)						
V_{DREF} Bias Current				0.6/R_{IREF}		A
Fast Start Threshold (VST)						
VST Bias Current				0.6/R_{IREF}		A

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX23224 MIN	LX23224 TYP	LX23224 MAX	UNIT
TTL INPUTS (EN_BLU,DIGITAL_DIM)						
Input Logic High	V_{IH}	Input Condition	2.0			V
Input Logic Low	V_{IL}	Input Condition			0.8	V
Input High Current	I_{IH}	V_{INH} = 5V			10 (140 for EN_BLU)	µA
Input Low Current	I_{IL}	V_{INL} < 0.8V			5 (25 for EN_BLU)	µA
Input Hysteresis Voltage	V_{IHH}			0.6		V
CMOS I/O (PS_SYNC/CLK)						
Input Logic Threshold	V_{TH}			V_{DD} *0.5		V
Output High Voltage	V_{OH}	I = 5mA	V_{DD} -0.5			V
Output Low Voltage	V_{OL}	I = 5mA			0.5	V
Over voltage protection (OVP1)						
OVP threshold	V_{IN_OVPT}		3.8	4	4.2	V
OVP Hysteresis	V_{IN_OVPH}			0.6		V
Under voltage protection ($V_{IN\ UVLO}$)						
UVLO Threshold Level	V_{IN_UVLOT}	Disable IC by holding POR low while under this level	3.85	4.0	4.2	V
UVLO Hysteresis	V_{IN_UVLOH}	Hysteresis for programmable input (V_{IN}) UVLO threshold level		0.5		V

PARAMETER	SYMBOL	TEST CONDITIONS / COMMENT	LX23224 MIN	LX23224 TYP	LX23224 MAX	UNIT
Open drain (FAULT)						
Output Low Voltage	V_{OL_FAULT}	I_{OL} = 2mA			0.2	V
Leakage Current	I_{L_FAULT}	V_{OUT} = 5V			1	µA
Threshold Voltage			2.4	2.5	2.6	V
Thermal Protection						
Over Temperature Shutdown	T_{SHUT_OFF}	Maximum temperature shutdown protection	160	175	195	ºC
Over Temp Shutdown Hysteresis	T_{OTSH}			40		ºC

Note: Thermal protection shuts down all DC/DC ports in auto restart mode; this mode is independent of the fault mode selection.

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

Pin Description

PIN DESCRIPTION				
QFN Pin #	SSOP Pin #	Pin Name	Pin Type	Description
1	7	COMP1	Input	DC/DC1 loop compensation, R/C network to PGND1
2	8	LED_ISNS1	Input	LED String1 current sense, resistor to PGND1. $R_{sense} = 0.35V/I_{LED}$
3	9	LED_STR1	Output	LED string1 NFET gate control
4	10	VD1	Input	Connect to an isolating NFET or diode to sense String 1 NFET drain voltage.
5	11	VD2	Input	Connect to an isolating NFET or diode to sense String 2 NFET drain voltage.
6	12	LED_STR2	Output	LED String2 NFET gate drive.
7	13	LED_ISNS2	Input	LED String2 current sense, resistor to PGND1. $R_{sense} = 0.35V/I_{LED}$
8	14	SL_COMP	Input	DC/DC boost converter slope compensation, resistor to AGND. $R_{SL\_COMP} = 1.2V/(10*m_a*30pF)$
9	15	V_{ST}	Input	DC/DC fast start threshold, resistor to AGND. Fast start stops when the OVP pin reaches VST. $R_{VST} = V_{ST} *R_{IREF}/0.6V$
10	16	SCD	Input	LED short circuit threshold, resistor to AGND. $R_{SCD} = V_{SCD}*R_{IREF}/2.4V$
11	17	VD_REF	Input	V_{DMIN} set point, resistor to AGND. $R_{VD\_REF} = V_{DMIN}*R_{IREF}/0.6V$
12	18	IREF	Input	Bias current setting, connect 30.1kΩ to AGND.
13	19	PS_OSC	Input	DC/DC frequency setting, resistor to AGND. $R_{PS\_OSC} = 9.7*(1000/F_{DC/DC} – 0.231)$ R_{PS_OSC} in kΩ and $F_{DC/DC}$ in kHz. Leave PS_OSC pin open to use an external clock.
14	20	AGND	Ground	Analog ground supply.
15	21	PS_SYNC/CLK	Input/Output	DC/DC clock output as a master of clock input as a slave.
16	22	FAULT	Output	Fault flag and hiccup timer, open drain, connect to an external R-C pull up network. Goes low to indicate a fault.
17	23	V_{DD}	Power	5V volt supply for internal circuitry, 2.2uF capacitor to AGND to guarantee stability.
18	24	EN_BLU	Input	Back light enable. Turns on the DC/DC converters and LED string controllers.
19	25	M0	Input	Test-only pin. Leave open.
20	26	DIGITAL_DIM1	Input	Digital Dimming Input
21	27	LED_ISNS4	Input	LED String4 current sense, resistor to PGND2. $R_{sense} = 0.35V/I_{LED}$
22	28	LED_STR4	Output	LED String 4 NFET gate drive
23	29	VD4	Input	Connect to an isolating NFET or diode to sense String 4 NFET drain voltage.
24	30	VD3	Input	Connect to an isolating NFET or diode to sense String 3 NFET drain voltage.
25	31	LED_STR3	Output	LED String 3 NFET gate drive

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

26	32	LED_ISNS3	Input	LED String3 current sense, resistor to PGND2. R_{sense} = 0.35V/I_{LED}
27	33	PGND2	Ground	Power ground for LED strings 3 and 4
28	34	V_{HS}	Output	Bias for internal PFET gate drivers, bypass with 1µF capacitor connected between this pin and V12V
29	35	V_{12V}	Power	12V supply voltage, bypass with 4x2.2µF capacitors connected between this pin and GND plane
30	36	V_{12VC}	Output	Control output to drive an external transistor to generate V12V. Bypass with 1µF capacitor to AGND. If internal regulation is used, connect to V_{12V} pin.
31	1	V_{IN}	Power	High voltage supply for the 12V regulator and housekeeping bias circuitry.
32	2	V_{IN_UVLO}	Input	Monitors V_{IN} through an external resistive voltage divider. If this function is not used connect to V_{DD}
33	3	PGND1	Ground	Power ground supply for DC/DC and strings 1 and 2.
34	4	GATE1	Output	DC/DC NFET gate control
35	5	DC_ ISNS1	Input	DC/DC NFET current sense
36	6	OVP1	Input	DC/DC over voltage protection threshold, connect to resistor divider between V_{boost} and PGND1.

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

Functional Description

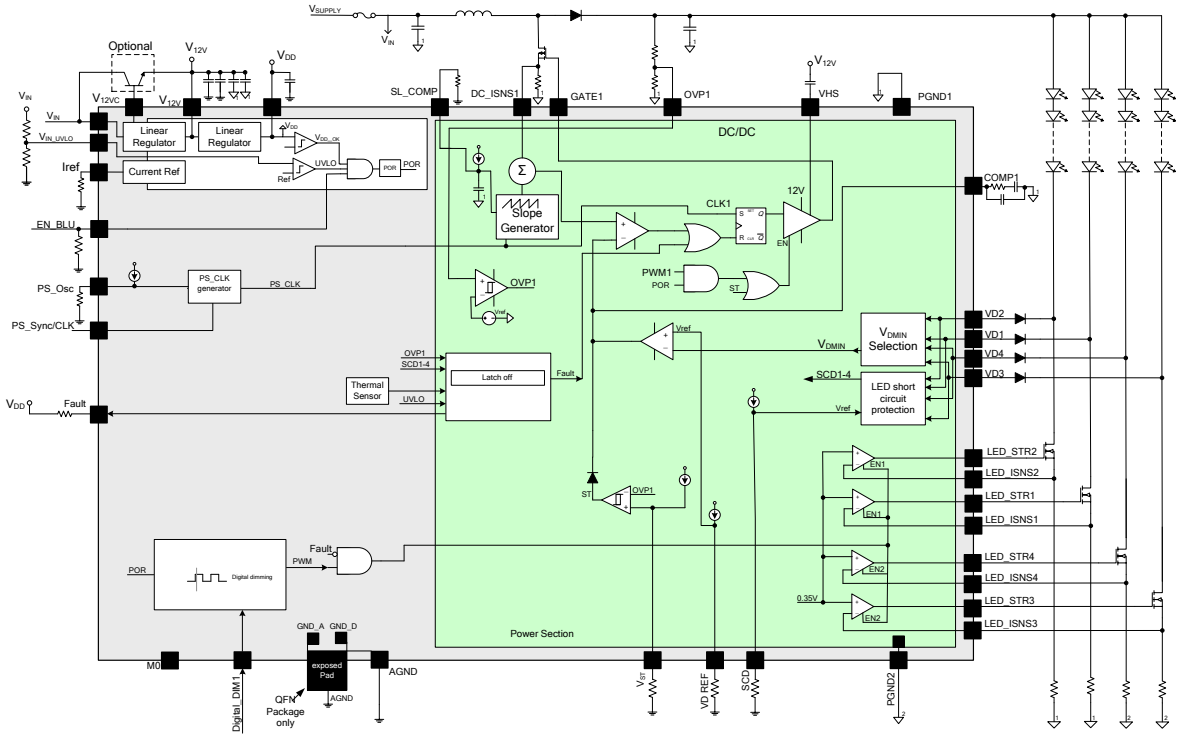


Figure 3: Functional Block Diagram

Theory of Operation

LX23224 controls four LED strings for a D0 edge LED BL LCD TV application. All four LED strings share a dedicated DC/DC switch mode current programmed controller. Switching converter can operate in a boost topology with fixed switching frequency in a range of 100 kHz to 300 kHz.

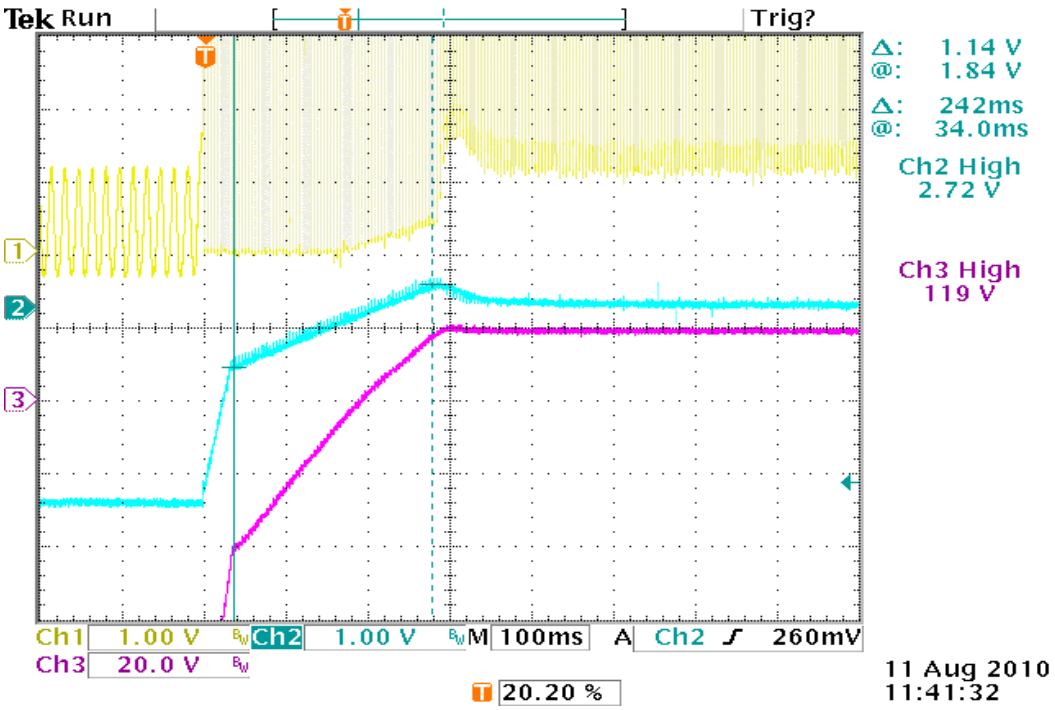
Start Up

When V_{IN} is applied, the internal 12V and 5V linear regulators and the bias voltage and current generators turn on. When all the regulators and bias voltages have stabilized above their respective UVLO thresholds, the LX23224 is ready to drive the LED strings. When the V_{IN_UVLO} and EN_BLU rising thresholds are met, the LX23224 starts switching at the DC/DC converters.

When the OVP voltage is below the V_{ST} voltage, the DC/DC converter will be continuously enabled. This allows the boost or flyback voltage to charge up quickly with no dependency on the PWM duty cycle. Above the V_{ST} voltage, the DC/DC converter switches only when the PWM signal is asserted. The V_{ST} voltage should be selected so that it is as high as possible but always lower than the normal boost or flyback voltage range. This will give the quickest start up performance.

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

Here is a picture of the start up sequence at 10% PWM duty cycle. Channel 1 is the NFET drain voltage, channel 2 is the COMP1 voltage, and channel 3 shows the boost1 voltage.



Input under Voltage Lock out Circuit (V_{IN_UVLO})

Input UVLO prevents the LX23224 from starting up in case the V_{IN} input voltage is lower than a user defined threshold. Connect a voltage divider on the DC/DC input voltage and set it according to the minimal requested system operating input voltage.

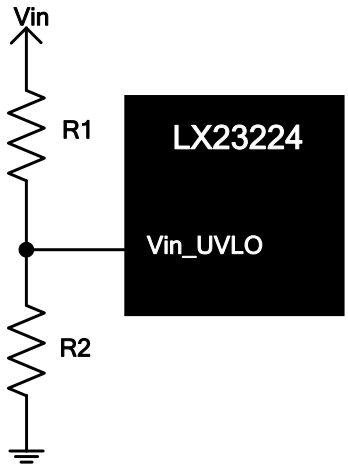


Figure 4: V_{IN_UVLO} Connection Example

2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

LED NFET Drain Voltage Measurements

The LX23224 regulates the DC/DC output voltage so that the lowest NFET drain voltage matches the target value as set by VD_REF pin. This target voltage should be selected so that the LED MOSFETs remain in their saturated region. Keeping this voltage as low as possible maximizes the system's power efficiency.

The LED MOSFET drain voltages are monitored through blocking diodes or blocking NFETs to protect the LX23224 from excessive voltages. ~90µA is sourced from each of the VD1-4 pins to bias external blocking diodes. If a blocking diode is used, then the voltage at the VD1-4 pins will be one diode drop above the actual LED NFET drain voltage. This voltage drop can be compensated for by raising VD_REF pin by a matching diode voltage drop.

A four input comparator determines which of the four drain voltage is lowest (V_{DMIN}). That voltage is then routed to the DC/DC error amplifier. The DC/DC control loop works to keep V_{DMIN} equal to VD_REF.

Power/Thermal Conditions

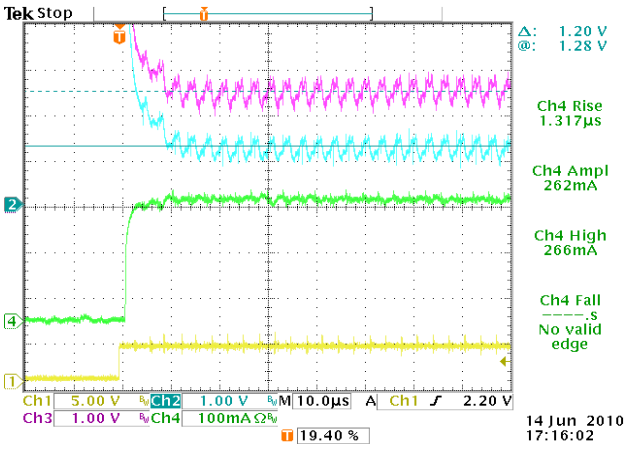
The maximum LED current depends on heat sink capabilities of the external LED's MOSFETs and the allowable temperature rise.

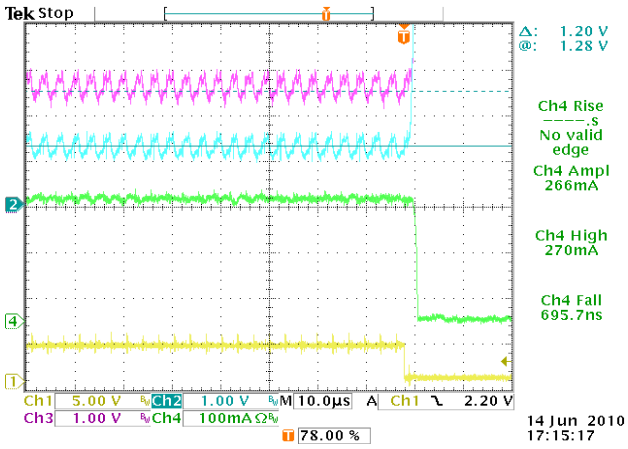
LED string current control

The LED string NFET is controlled by the LED_STR pin so that the voltage at the LED_ISNS pin is 350mV when a string is enabled by the DIGITAL_DIM input going high. At the rising edge of the PWM signal, the LED_STR pin is quickly charged up to turn on the LED NFET. When the PWM signal is deasserted, the LED_STR pin is quickly discharged to 0V.

When the LED string is turned on, the NFET drain voltage quickly drops from the boost voltage to around 1V. It can take up to 20uS for the drain voltage to stabilize. It also takes around 3 to 4 PS clock periods for the boost inductor to charge to its steady state value. For this reason, a 10uS blanking period is used at the leading edge of the PWM signal to keep the drain voltage control loop from being disturbed. For the same reason, it is recommended that the minimum PWM pulse be greater than 20uS.

Here are pictures showing the beginning and end of a digital PWM pulse. Channel 1 = DIGPWM, Channel 2 = Vdrain1, Channel 3 = Vdrain2, Channel 4 = LED String 2 current. These pictures show how the minimum drain voltage is regulated to about 1V. The ripple on the drain voltage is due to the ESR ripple from the boost power supply. The high impedance nature of the LED current source works to reject this voltage ripple from affecting the LED string current.





2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

DC/DC boost controller

The LX23224 DC/DC boost converters operate at a constant frequency with peak current control. The minimum output pulse width is 100nS. Once started, the output pulse will terminate immediately when any of the following events occur:

- The DC_ISNS voltage crosses 200mV.
- The DC_ISNS voltage plus the artificial slope compensation crosses the DC/DC comparator control voltage (Vc). Vc is derived from the COMP pin via a level shift and a 5:1 attenuator.
- Maximum duty cycle has been reached. In boost mode, the maximum duty cycle is set to 90%.

PS Switching Frequency Set (PS_OSC)

DC/DC switching frequency and operation mode are set by a resistor at PS_OSC pin. Frequency can be programmed from 100 kHz to 300 kHz.

R_{osc}	DC/DC FREQUENCY	IC MODE
95.3kΩ ≥ R_{PS-OSC} ≥ 30.1kΩ	100kHz ≤ f_{OSC}≤ 300kHz	Asynchronous or Master mode
open	Not applicable	Slave mode

Note: To disable DC/DC oscillator for synchronizing it with another LX23224 functioning as a "Master", R_{PS-OSC} should be left open (see PS_SYNC/CLK pin description).

PS Clock Synchronization (PS_SYNC/CLK)

PS_SYNCH/CLK input/output is used to synchronize DC/DC converters between two LX23224 drivers within a single system.

When using two LX23224s, DC/DCs can operate in asynchronous or synchronous modes

- Asynchronous mode – When utilizing two LX23224 LED drivers, each DC/DC works in an individual operating frequency.
- Synchronous mode – When utilizing two LX23224 LED drivers that work in the same frequency, one should be set as a master and the other one as a slave.
  Master setup: PS_OSC resistor set for the required frequency.
  Slave setup: PS_OSC resistor bigger than 1MΩ or not connected.
  PS_SYNC line should be connected between the two LED drivers.

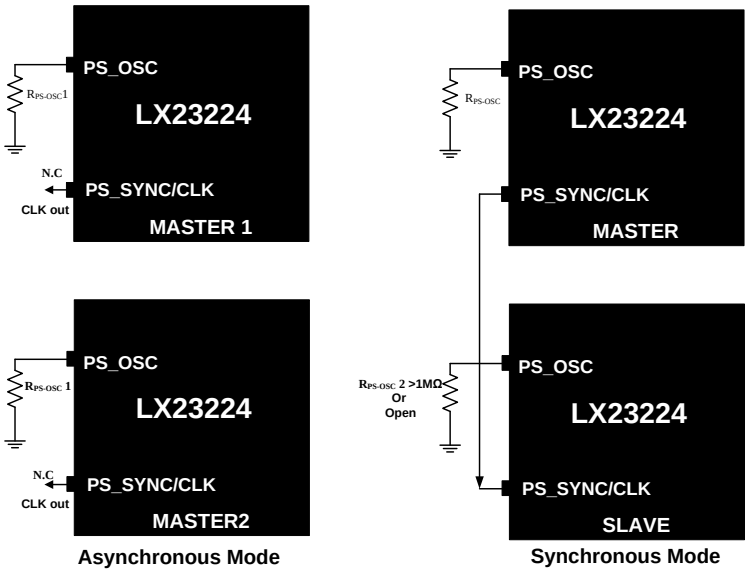


Figure 5: PS Asynchronous/synchronous Mode

DC/DC Start Up

There are two start up modes: Normal (slow) and Accelerated.

In Normal (slow) mode, start up time is a function of LED BL Dimming frequency and duty cycle, since LED PWM modulates DC/DC ON time.

In Accelerated mode, DC/DC starts up in open loop and operates in this mode until DC/DC voltage reaches about 80% of LED voltage (user selected). This value is programmed by a resistor connected to V_{ST}. After reaching this threshold, start up continues in normal mode, whereas DC/DC ON is modulated with PWM.

If V_{ST} pin is connected to ground, DC/DC starts up in a normal mode.
Accelerated mode significantly reduces the startup time difference, especially when LED's dimming is working in low duty cycle.

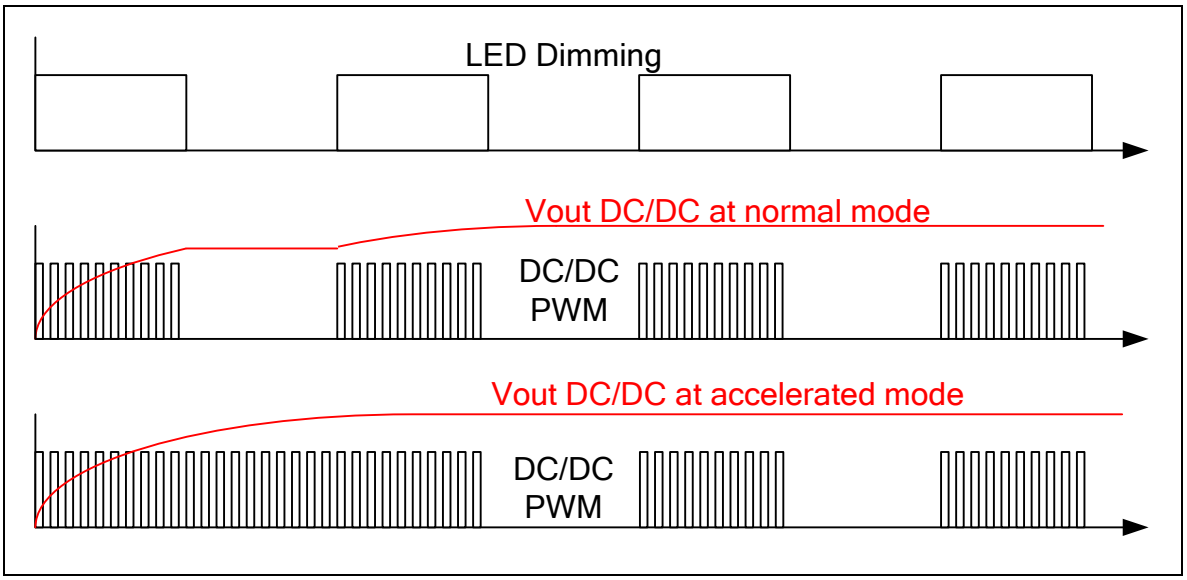


Figure 6: Normal/Accelerated Mode

Fault Events

LX23224 detects and protects against the following possible fault conditions:

- Over Voltage Protection of DC/DC #1 (sampled on OVP1)
- LED Short Circuit of Channel #1 (sampled on VD1)
- LED Short Circuit of Channel #2 (sampled on VD2)
- LED Short Circuit of Channel #3 (sampled on VD3)
- LED Short Circuit of Channel #4 (sampled on VD4)
- Open LED of Channel #1 (Sampled on VD1)
- Open LED of Channel #2 (Sampled on VD2)
- Open LED of Channel #3 (Sampled on VD3)
- Open LED of Channel #4 (Sampled on VD4)
- V_{in} under Voltage (Sampled on V_{IN_UVLO})
- IC Thermal Protection

LED short circuit conditions are detected by monitoring LED MOSFET drain voltages. When the difference between MOSFET drain voltages for a LED string pair (VD1-VD2 or VD3-VD4) exceeds the level of four times the voltage at SCD pin, a short circuit event is declared.

LED open circuit conditions are detected by a combination of OVP pin and VD pins. When a LED string is open the corresponding VD voltage changes to 0V. This causes the DC/DC loop to pump up the boost voltage. The high boost voltage will most likely cause the drain voltage of the non-open string to rise above short circuit detection level. This will cause a short circuit event to be declared. If both LED strings are open boost voltage will rise until it hits OVP protection threshold and an OVP event is declared.

Thermal and V_{IN_UVLO} shutdown functions are an auto-restart mode. That means after IC temperature drops below thermal protection limit (see Electrical Characteristics table) or input voltage rises above UVLO protection threshold, the system automatically turns on, all others faults will latch off LED drivers and DC/DC. If IC temperature reaches thermal shutdown limit, the DC/DC shuts down and a fault signal is transmitted.

Typical Powering Schemes

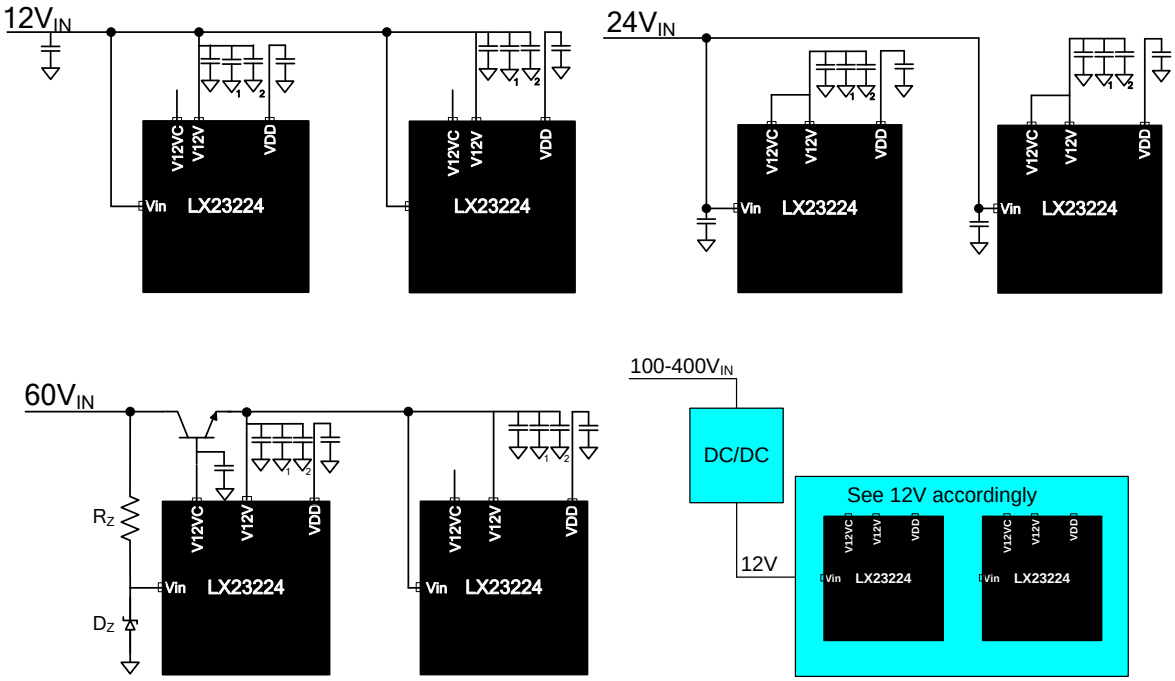


Figure 7: Powering Diagram

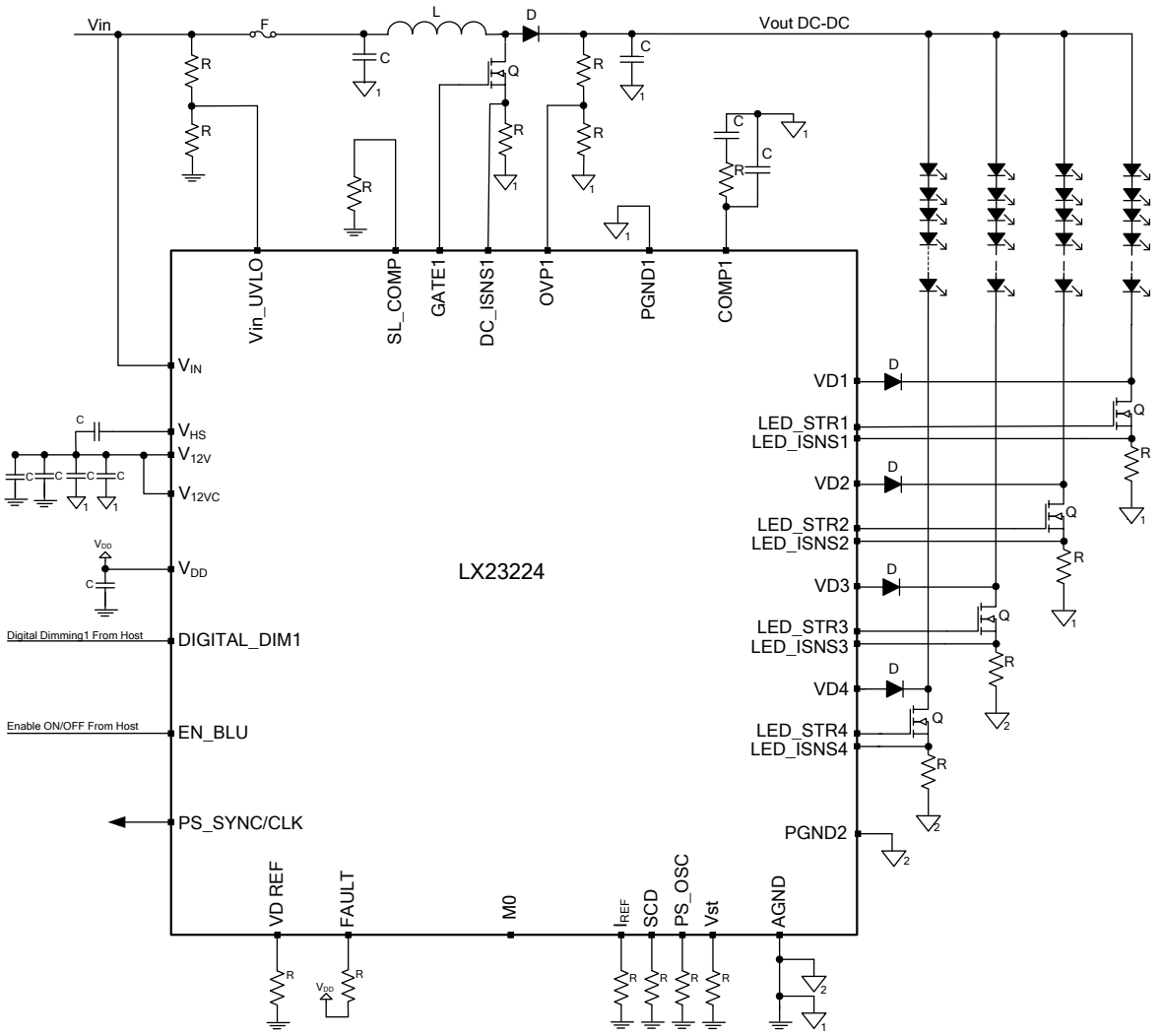


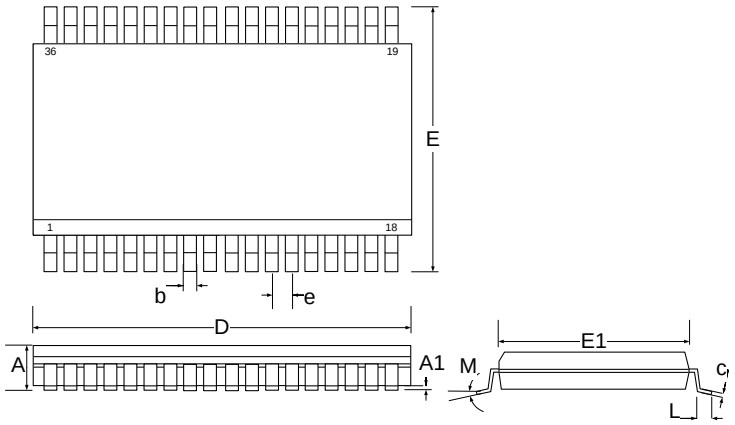
Figure 8: Typical Application Diagram

Microsemi
Analog Mixed Signal Group
2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

PACKAGE DIAGRAM

DB

36-Pin Small Shrink Outline Package (SSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.44	2.65	0.096	0.104
A1	0.10	0.30	0.004	0.012
b	0.25	0.51	0.010	0.020
c	0.20	0.33	0.009	0.013
D	15.20	15.60	0.598	0.614
E	10.05	10.55	0.396	0.415
E1	7.40	7.60	0.291	0.299
e	0.80 BSC		0.031 BSC	
L	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
*LC	–	0.10	–	0.004

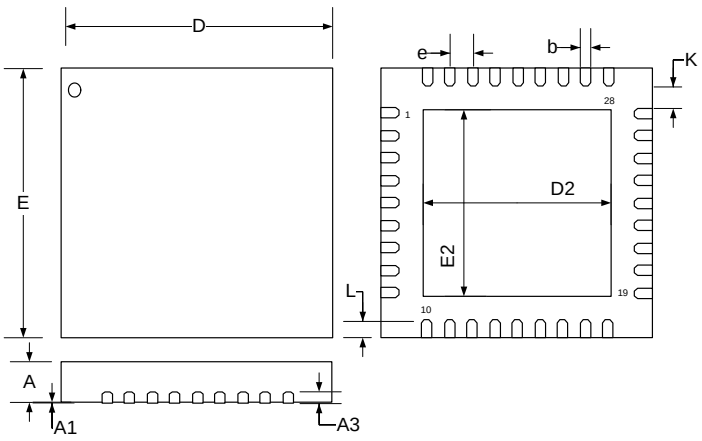
*Lead Coplanarity

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

LQ

36-Pin QFN 6x6mm



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.45	0.65	0.018	0.025
b	0.18	0.30	0.007	0.012
D2	4.00	4.25	0.157	0.167
E2	4.00	4.25	0.157	0.167
D	6.00 BSC		0.236 BSC	
E	6.00 BSC		0.236 BSC	

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Microsemi
Analog Mixed Signal Group
2381 Morse Avenue, Irvine, CA 92614, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / Dec 2010		Preliminary Release
1.0 / July 2011		Release to Production
1.1 / July 2011		Adjust specs

For support contact: sales_AMSG@microsemi.com

Visit our web site at: www.microsemi.com

Catalogue Number: DS_LX23224