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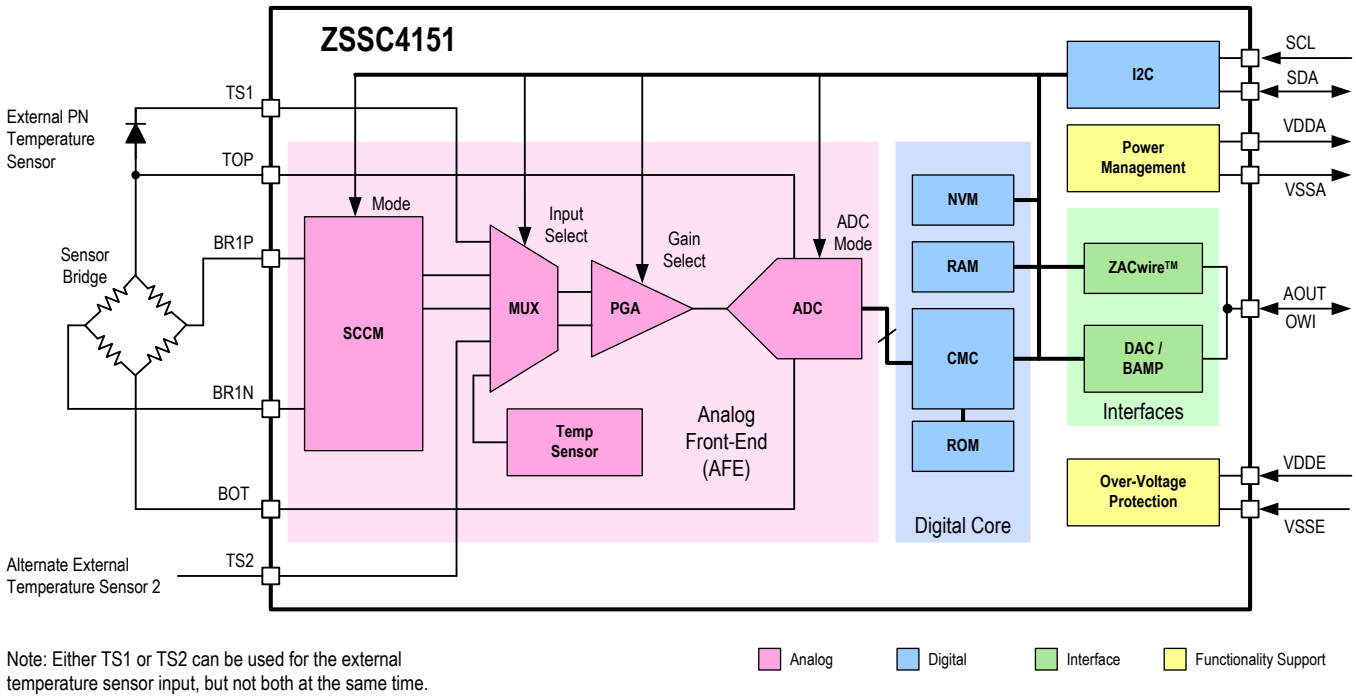
1. Introduction

The signal path of the ZSSC4151 circuits consists of the analog front-end (AFE), the digital signal processing unit (CMC), the overvoltage protection circuitry, the ZACwire™ one-wire interface (OWI), and the analog output (AOUT). An optional I2C interface is available for calibration and evaluation. A single set of differential inputs (BRP and BRN pins) are inputs from the sensor bridge. The differential input is handled by two signal lines, each with a dynamic range symmetrical to the common mode potential (analog ground is equal to VDDA/2) so that it is possible to amplify positive and negative input signals within the common mode range of the signal input. The input signals used are selected by the input multiplexer.

Figure 1.1 Block Diagram of the ZSSC4151



Note: Either TS1 or TS2 can be used for the external temperature sensor input, but not both at the same time.

Abbreviations:

SCCM	Sensor Check and Common Mode Adjustment Unit
MUX	Multiplexer
PGA	Programmable Gain Amplifier
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
RAM	Volatile Memory for Configuration and Conditioning Coefficients
ROM	Read-Only Memory for Correction Formula and Algorithm
NVM	Non-volatile Multiple-Time Programmable (MTP) Memory for Configuration and Conditioning Coefficients
DAC/BAMP	Analog Output Stage
I2C	I2C Digital Interface

The multiplexer (MUX) transmits the input signals, which can be from a bridge sensor, a selected temperature sensor, or diagnostic voltage levels (see section 2), to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensor signal can be from the internal PTAT source, external diode, external PTC-type RTD sensors, or the sensor bridge as selected by the configuration programmed in NVM via the ZSSC4151 Evaluation Kit Software, also referred to as the graphical user interface (GUI). The multiplexer can support differential or single-end sensor inputs; however, it converts single-ended inputs to differential signals for signal processing. The differential signals are pre-amplified by the programmable gain amplifier (PGA). The ADC converts these signals into digital values.

The digital signal correction is processed in the calibration microcontroller (CMC) using a set of selectable ROM-resident correction formulas and sensor-specific coefficients stored in the NVM during calibration. The configuration data and the correction parameters can be programmed into the NVM via the digital OWI communication at the output pin or by digital communication via the I2C interface. During the calibration procedure, the digital interfaces can also provide measurement values.

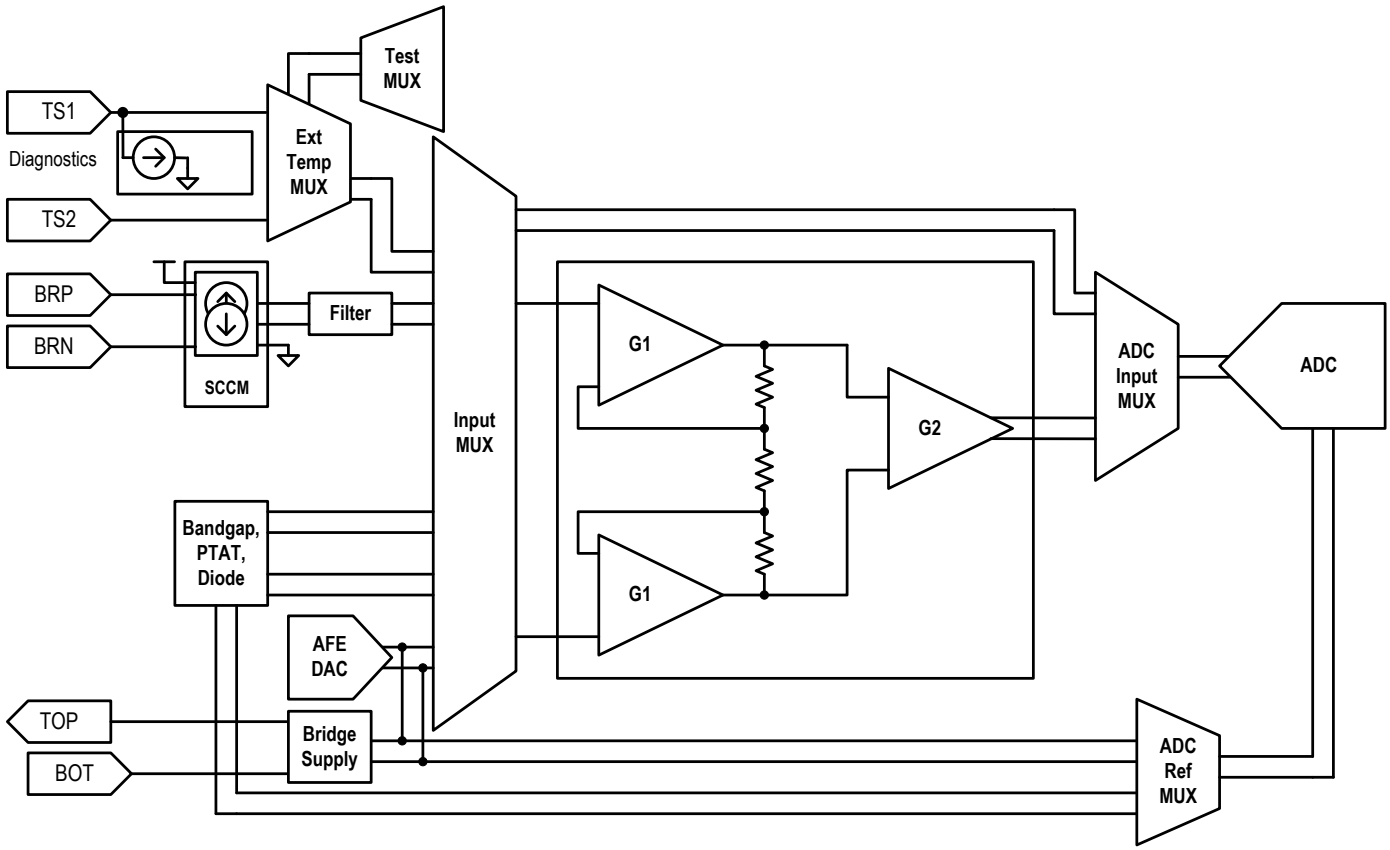
2. AFE

The analog front end (AFE) consists of the sensor connection check module (SCCM), the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC).

2.1 Sensor Check and Common Mode Adjustment Unit (SCCM)

The SCCM block contains the circuitry needed to test the sensor inputs for fault conditions. The sensor check detects both shorts and opens. The SCCM has programmable probe currents used during diagnostic checks to account for different sensor types. In addition, the SCCM has an analog front-end digital-to-analog converter (AFEDAC) that can supply diagnostic voltages.

Figure 2.1 Analog Front End (AFE) Block Diagram



2.2 Programmable Gain Amplifier (PGA)

The programmable gain amplifier (PGA) is a two-stage amplifier with gain settings configurable via the GUI as listed in Table 2.1. This is the analog coarse gain adjustment before the signal is input to the ADC. There is also a digital fine gain adjustment as part of the digital calibration. The digital gain supports both positive and negative gain settings configured via the GUI to achieve the highest possible span.

Table 2.1 Gain Settings

Option	Gain	First G1 Stage	Second G2 Stage	Maximum Input Span V_{IN_SPAN} (mV/V) [a]	Input Common Mode Range V_{IN_CM} (% VDDA)
0	1	1	1.00	800	5 to 95
1	1.4	1	1.56	578	30 to 65
2	2.1	2	1.11	385	30 to 65
3	3.15	2	1.56	254	30 to 65
4	4.3	2	2.21	186	30 to 65
5	6.25	2	3.13	128	30 to 65
6	8.3	8	1.11	96	30 to 65
7	12.6	8	1.56	63	30 to 65
8	17.3	8	2.21	46	30 to 65
9	25.0	8	3.13	32	30 to 65
A	33.2	32	1.11	24	30 to 65
B	50.4	32	1.56	16	30 to 65
C	69.0	32	2.21	12	30 to 65
D	100.0	32	3.13	8	30 to 65
E	138.0	64	2.21	6	30 to 65
F	200.0	64	3.13	4 [b]	30 to 65

[a] The internal limitation for the gain is the ADC input, which is limited to 10% to 90% of the ADC reference (example: VDDA – VSSA). The recommended internal signal range maximum is 80% of the VDDA voltage. The span is calculated by the following formula: span = 80% / gain.

[b] Digital zooming allows reducing the input span depending on application the requirements.

Table 2.2 SCCM Settings in the GUI

SCCM Settings	Option	Description
Current Mode		
Probe Current	0	6.25µA
	1	25µA
	2	100µA
	3	400µA
Current Cross	0	Sink/source current at the same node
	1	Sink/source current at opposite pin BRP/BRN
Current Output	0	Disable
	1	Enable
Current Sink	0	Source current reference in current comparator
	1	Sink current reference in current comparator
Current Injection Polarity	0	Sink current at pin BRP
	1	Sink current at pin BRN
Sensor Connection Check	0	Disable
	1	Enable
Current Mode Diagnostics Activated for Bridge	0	Disable
	1	Enable
Voltage Mode		
Reference Select	0	TOP and BOT pins as DAC reference
	1	VDDA and VSSA pins as DAC reference
Reference Voltage	0	0.1111111111 ∗ (TOP – BOT) or (VDDA – VSSA)
	1	0.2222222222 ∗ (TOP – BOT) or (VDDA – VSSA)
	2	0.3333333333 ∗ (TOP – BOT) or (VDDA – VSSA)
	3	0.4444444444 ∗ (TOP – BOT) or (VDDA – VSSA)
	4	0.5 ∗ (TOP – BOT) or (VDDA – VSSA)
	5	0.5555555556 ∗ (TOP – BOT) or (VDDA – VSSA)
	6	0.6666666667 ∗ (TOP – BOT) or (VDDA – VSSA)
	7	0.7777777778 ∗ (TOP – BOT) or (VDDA – VSSA)

2.3 Multiplexer (MUX)

The multiplexer (MUX) allows many combinations of different inputs to the ZSSC4151 through either external pins or internally connected signals. Table 2.3 lists the different multiplexer options. The MUX selects both the negative and positive inputs of the differential signal paths as well as assigning the inputs for the internal measurement tasks running in the measurement cycle.

These options allow defining the bridge input polarity as well as the source of temperature for the bridge measurement compensation. See Figure 2.1 for an illustration of the possible multiplexer inputs.

Table 2.3 MUX Channels

Note: Settings shaded gray in this table are not applicable to the ZSSC4151 or are reserved for IDT internal use.

Option	MUX Channel	Use Cases [a]	Description
0	BR1P	Bridge polarity inversion	Main channel bridge positive input.
1	BR1N		Main channel bridge negative input.
2	BR2P	Reserved for IDT internal use only.	Main channel bridge positive input.
3	BR2N		Main channel bridge negative input.
4	AFEDACP	External temperature sensor	Analog front-end DAC (AFEDAC) positive input (see Figure 2.1).
5	AFEDACN	Reserved for IDT internal use only.	Analog front-end DAC (AFEDAC) negative input.
6	PTATP	Internal temperature sensor	High accuracy internal temperature sensor; this temperature sensor is diode-based (both inputs must be selected simultaneously).
7	PTATN	Internal temperature sensor	
8	VDC	Reserved for IDT internal use only.	Internal supply voltage for control circuitry in analog domain (use for testing only).
9	DION		**Important:** Reserved for IDT use only. Do not select.
A	TOP		Voltage from TOP pin.
B	TS1	External temperature sensor	External temperature input 1. For an external diode, measure against TOP. For an external RTD (PTC only), measure against AGND (internal ground).
C	TS2	External temperature sensor	External temperature input 2. For an external RTD (PTC only), measure against AGND.
D	AGND	Reserved for IDT internal use only.	Internal analog ground or ½ (VDDA – VSSA).
E	VDD		Digital supply voltage 1.8V typical (for test only).
F	VSSA		Analog negative supply; normal operation = 0V.

[a] Uses cases describe the usage of the input multiplexer selection in a final application. This is used for flipping bridge polarity as well as selecting the temperature source for the bridge compensation calculations.

2.4 Analog-to-Digital Converter (ADC)

2.4.1 General Overview

The analog-to-digital converter has a two-stage charge-balance architecture. The resolution is configurable from 12 to 18 bits via the NVM configuration. An inherent range shift at the ADC can also be set. The ADC resolution and range shift settings can be used to optimize the bridge measurement. All other measurements have fixed settings and thus timing for them depends entirely on the ZSSC4151 configuration.

The analog-to-digital (A/D) conversion raw measurement results are stored in the RAM output memory as a signed 16-bit value (sint16). Equation 1 illustrates the conversion of a single measurement task. Each measurement task in the measurement cycle will use this equation to convert the input signal from the multiplexer to a digital value.

Note: Regardless of the ADC resolution setting, the raw measurement result is always 15 bits plus a sign bit. For resolutions less than 15 bits, the values are always stored left-aligned in the register as shown in Figure 2.2. For resolutions above 15 bits, which are typically used for sensors with a large DC offset, digital zooming is required (refer to the *ZSSC415x Application Note – ZSSC4151 ADC Segmentation*). In this case, the additional LSBs are stored in a secondary register. The results maintain the original resolution setting of the A/D conversion and enable compensation for small signals with large DC offsets.

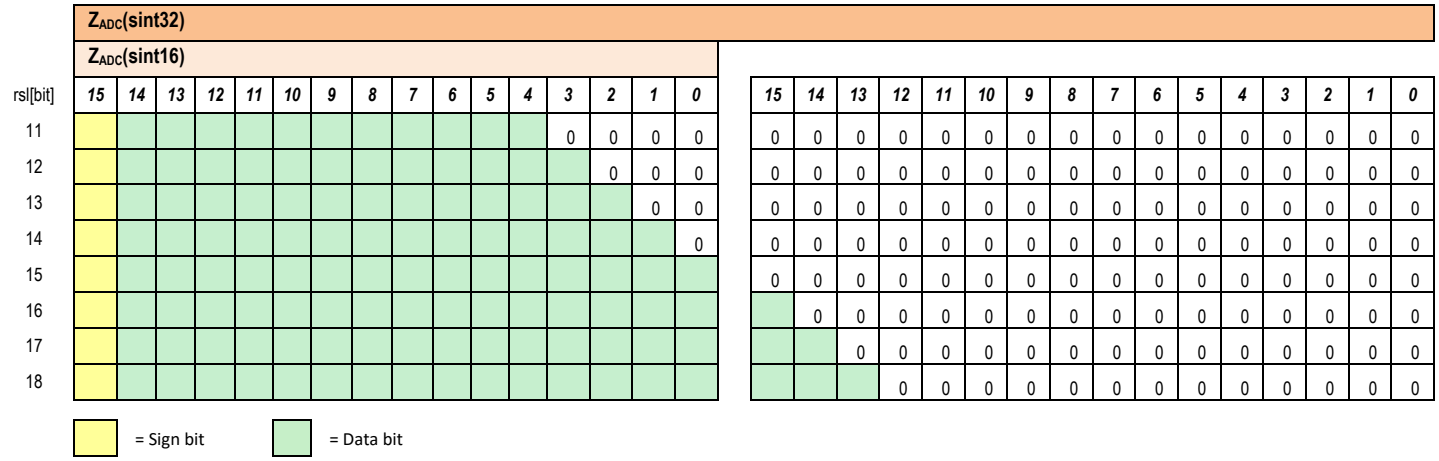
$$Z_{ADC} = \left(\frac{gain * (V_{IN\_DIFF} + V_{OFFSET})}{ADC_{REF}} + adcRngShift - zoom \right) * 2^{15+scale} \qquad \textbf{Equation 1}$$

Where

Z_{ADC}	Output counts of ADC
V_{IN_DIFF}	Differential input voltage at bridge input pins
V_{OFFSET}	AFE offset voltage
gain	AFE gain: 1 to 200
ADC_{REF}	ADC reference voltage: VDDA or TOP/BOT
adcRngShift	ADC range shift: 1/16, 1/8, 1/4, or 1/2 (see section 2.4.3)
R_{ADC}	Resolution of A/D conversion: 12 to 18
zoom	Zooming offset: 0, 1/16, 2/16, 3/16, … 15/16 (for details, see the *ZSSC4151 Application Note – ADC Segmentation*)
scale	Max [0: (R_{ADC} – 15)]: 0, 1, 2, or 3

The Z_{ADC}*(sint16)* measurement value is used by the 16-bit CMC for conditioning operations. The measurement value can be directly read from the RAM output memory. In addition, the Z_{ADC}*(sint32)* value is stored in the RAM output memory for configurations with an A/D conversion higher than 15-bit. A 16-bit section can be selected from this Z_{ADC}*(sint32)* value using the *zoom* parameter. The signed format is necessary because the automatic offset compensation (*AZ measurement*) can produce negative measurement results, depending on the signal.

Figure 2.2 ADC Measurement Result Format



2.4.2 ADC Resolution

Table 2.4 lists the ADC resolution settings available for the ZSSC4151 with the resulting ADC conversion time, illustrating the trade-offs between resolution and timing. Increasing the number of MSBs will result in a more precise measurement; however, this will increase the integration time of the A/D conversion. Since the CMC will use internal 16-bit signed registers, ADC resolutions greater than 15 bit require the ADC zooming function.

Table 2.4 ADC Example Settings

Note: See important notes at the end of the table.

Note: Settings shaded blue in this table support digital zooming to correct sensor signals with a large offset. For more about digital zooming and MSB/LSB resolution, refer to the *ZSSC415x Application Note – ZSSC4151 ADC Segmentation*.

Resolution	ADC MSB Resolution	ADC LSB Resolution	ADC Conversion Time(µs) [a]
12	8	4	208
	9	3	352
13	8	5	208
	9	4	352
	10	3	640
14	8	6	208
	9	5	352
	10	4	640
	14	0	9280
15	8	7	208
	9	6	352
	10	5	640
	11	4	1216
	12	3	2368

Resolution	ADC MSB Resolution	ADC LSB Resolution	ADC Conversion Time(µs) [a]
16	8	8	272
	9	7	352
	10	6	1216
	11	5	2368
17	9	8	416
	10	7	640
	11	6	1216
	12	5	2368
	14	3	9280
18	9	9	544
	10	8	704
	11	7	1216
	12	6	2368
	14	4	9280

[a] **Important:** IDT has measured the conversion time with the following preconfigured settings, which must not be changed by the user: AFE chopper length = 64, ADC MSB phase clock divider = 2, ADC clock divider = 2, ADC LSB conversion overlap enabled, ADC chopper break length = 64, ADC MSB pre-phase length = 32, AFE pre-phase length factor = 16, and clock = 8MHz.

2.4.3 ADC Range Shift

Another option available to the ADC is the range shift feature. The ADC range shift setting allows the ADC input to adjust to offsets in the bridge input signal. The ADC range shift can be set to capture the maximum span of the incoming signal when combined with the PGA gain, which is used to maximize the sensing element's signal span. Once the measurement is in the digital domain, a digital gain and offset can be used to achieve the full output resolution after calibration. The ADC shift is always shifting to the upper count range, so for negative offsets, it is necessary to switch the polarity of the bridge input. In this special case during calibration, the digital gain can be set to a negative value. This allows negative offsets to be removed via calibration while the signal remains in a range where the counts increase as the sensor signal increases.

Table 2.5 ADC Shift Settings

Setting	*adcRngShift* used in Equation 1	Description	ADC Output Counts with a 0mV Differential Input Signal [a]
-1/2 to +1/2	1/2	Centered in ADC range	16384 [4000_{HEX}]
-1/4 to +3/4	1/4	Shifted +25%	8192 [2000_{HEX}]
-1/8 to +7/8	1/8	Shifted +37.5%	4096 [1000_{HEX}]
-1/16 to +15/16	1/16	Shifted +43.75%	2048 [0800_{HEX}]

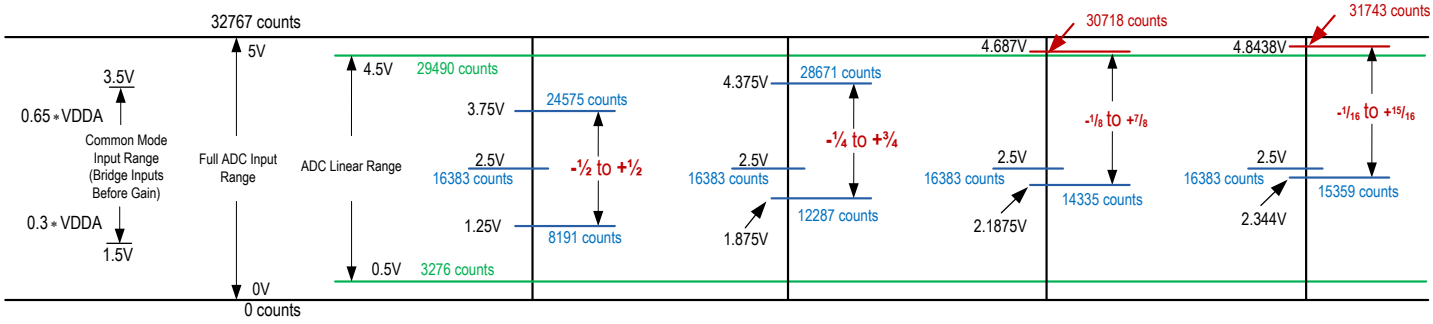
[a] This value can be shifted by the ADC digital measurement zooming offset (see the *zoom* parameter in Equation 1). This digital zooming is only required in the case when the sensing element has a signal offset that is close to or higher than the sensor signal span. In this case, the ADC resolution should be set to 16, 17, or 18 bit.

If the differential input signal is equal to 0mV, this ADC output count is generated. A differential input value of 0mV can be caused by setting the multiplexer to the same input data as is specified for auto-zero measurements.

Note: When adjusting the ADC shift and analog gain, stay within the linear range of the ADC input (10 to 90%).

The ADC operates in the differential mode centered on the common mode voltage. Figure 2.3 shows the effects of the different settings for the ADC range shift for an example when the ADC input signal span is 2.5V and the full ADC input range could cover 5V input range.

Figure 2.3 ADC Shift Settings Example using a 2.5V Signal Span



Note: In this example, the positive sensor input is always ≥ the negative input, the ADC = 15 bits + sign, and the reference to ADC is 5V/0V.

3. Calibration Microcontroller (CMC)

3.1 Overview

The calibration microcontroller (CMC) is a 16-bit digital signal processor (DSP) with a 24-bit arithmetic logic unit (ALU). The CMC performs state machine functions for the device, calculations for temperature compensation, and formatting functions for the analog output interface.

Features configured through the CMC:

- Diagnostic options
- Selection of multiplexer inputs
- Measurement tasks for bridge, temperature, and diagnostics measurements
- Conditioning tasks that remove errors in the overall signal path due to DC offsets and temperature effects
- Format analog output in Normal Operation Mode (NOM)
- Format One-Wire Interface (OWI) and I2C communications in Command Mode or Diagnostic Mode

The calibration coefficients are unique for each sensor module after the ZSSC4151 has been mounted with the specific sensing element. Coefficients are determined during the calibration process and stored in the NVM memory. During calibration, the module's bridge and, if selected, the temperature data are collected at different input stimuli levels. The coefficients can be calculated using either the calibration screen in the GUI or using a *.dll* file provided by IDT.

3.1.1 General Working Modes

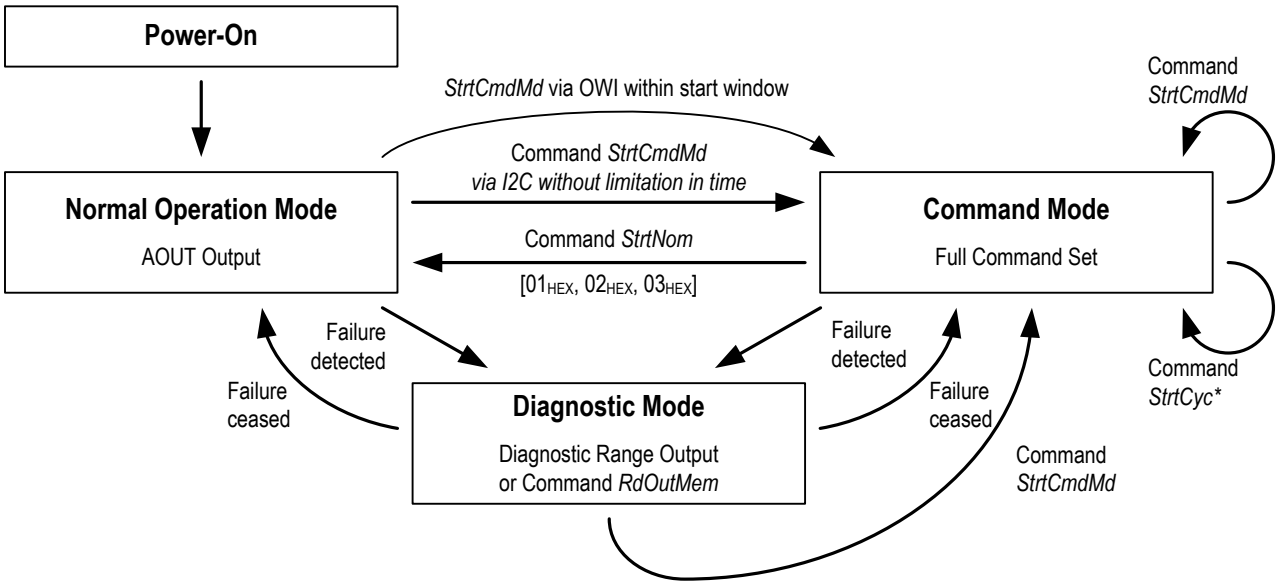
Figure 3.1 illustrates the available operation modes and transitions using a state diagram. Table 3.1 lists the commands used for changing from one state to another state.

Table 3.1 Command Set for Handling Operation Modes

Command Code	Command Name	Short Description
01_{HEX}	*StrtNom*	Start Normal Operation Mode
02_{HEX}	*StrtCycNvm*	Start the measurement and conditioning cycle from non-volatile memory (NVM)
03_{HEX}	*StrtCycShdw*	Start the measurement and conditioning cycle from shadow RAM
72_{HEX}	*StrtCmdMd*	Start Command Mode (authorization key: $F5A2_{HEX}$)

Figure 3.1 Operation Modes

Note: Refer to the *ZSSC4151 Commands* HTML file for descriptions of the commands shown here.



3.1.2 Normal Operation Mode

The Normal Operation Mode (NOM) is the recommended working mode for sensor applications. After power-on, the startup phase is processed. During this phase, the output is in tri-state. After the startup phase, the output buffer will be enabled; the output will be actively driven if enabled; and NOM starts automatically. Changing from NOM to Command Mode (CM) requires sending a special command and authentication code.

The startup phase includes the following steps:

- Settling phase for the internal supply voltage (i.e., the VDDA – VSSA potential), which ends when the reset signal is disabled through the power-on-reset block (POR). Refer to the *ZSSC4151 Application Note – Power Management and Fault Condition Protection* for power on/off thresholds.
- System initialization:
  - Clearing RAM
  - NVM CRC check
  - Mirroring ROM content to RAM
  - Mirroring non-volatile memory (NVM) content to RAM
- Completing the initial measurement cycle with a special startup configuration to get all the required measurements for the bridge conditioning calculation as early as possible.
- First conditioning calculation.
- Analog output of the first conditioned value depending on the AOUT output configuration (AOUT_CYC_WIN, AOUT_CYC, AOUT_WIN, or OWI; refer to section 5.1).

The NVM content, including its configuration and calibration data, is checked against the stored CRC. The configuration is activated and the measurement and conditioning cycle is started to process the sensor signal. If an internal check fails, then the ZSSC4151 will change to the Static Diagnostic Mode, which sets the analog output to the lower or upper diagnostic range depending on the NVM configuration. Refer to section 3.1.4.1 for details about Static Diagnostic Mode.

In NOM, the measurement cycle and the conditioning calculations that are predefined in NVM are processed continuously. The sensing element signal and the compensation temperature signal are measured; the conversion results are included in the conditioning calculation. The signal conditioning result is used to generate the analog output at the AOUT pin. In addition to the bridge and temperature measurements, the ZSSC4151 will perform built-in self-test (BIST) measurements for monitoring the complete sensor and ZSSC4151 system operation.

After power-on, there is a startup window during which the one-wire interface (OWI) can be used for optional communication via the AOUT pin. During the startup window, the output level at the AOUT pin depends on the selected output mode. See section 5.1 for details for the power-on behavior.

3.1.3 Command Mode

The Command Mode (CM) is the working mode that is used for calibration data acquisition and for access to the internal NVM of the ZSSC4151. The Command Mode start command *StrtCmdMd* aborts the running Normal Operation Mode (NOM) or Diagnostic Mode (DM), which stops the measurement and conditioning cycle. The analog output is disabled, and the AOUT pin is switched to the high-impedance OWI Mode.

The ZSSC4151 changes to CM only after receiving the command *StrtCmdMd* by one-wire communication (OWI) or I2C communication. Note that communication via OWI is only enabled during the startup window in NOM, and the *StrtCmdMd* is the only command accepted. This protects the ZSSC4151 against interruption of processing the measurement and conditioning cycle and against unintentional changes of the configuration. Note that the *StrtCmdMd* command can always be transmitted via I2C communication without any time limitation after power-on.

To start Command Mode, the OWI requires a special timing sequence and in some cases OWI driver capability. The OWI master must be able to fulfill two requirements:

- Control of the VDDE supply line to enable switching off VDDE and OWI. This enables the OWI Master to power down the ZSSC4151. This also allows controlling the time between powering up and sending the *StrtCmdMd* to meet startup window requirements.
- Capability to drive more than 20mA for OWI communication.

Since the ZSSC4151 can be programmed to provide analog output directly after the first valid measurement is available, ZSSC4151 and OWI master will both have access to the OWI communication line. Thus the OWI master must be able to bring the ZSSC4151 analog output stage into current limitation and thus allow OWI communication.

Details about the serial interface descriptions are provided in section 4.

In CM, the full set of commands is supported (see the *ZSSC4151 Commands* HTML file). Some commands need an additional authorization such as NVM write authorization. In addition to the commands overview (see *ZSSC4151 Commands*), a complete description of the command for particular calibration steps can be found in the *ZSSC4151 Support XLS Sheet* documentation.

3.1.4 Diagnostic Mode (DM)

The ZSSC4151 detects various possible failures, in which case the DM is activated. The DM is indicated by the ZSSC4151 setting the AOUT output pin in the diagnostic range. This can be either the low or high range. Typically, there are two main output ranges covering the following diagnostic ranges:

- Normal output range between 10 to 90% → Diagnostic range is from 0 to 8% and 92 to 100%
- Normal output range between 5 to 95% → Diagnostic range is from 0 to 4% and 96 to 100%

The ZSSC4151 differentiates between Static Diagnostic Mode and Temporary Diagnostic Mode. During Static Diagnostic Mode, the OWI interface will be enabled so that switching to CM is possible and so failure location can be determined.

3.1.4.1 Static Diagnostic Mode

If the Static Diagnostic Mode is activated, operation is affected as follows:

- The measurement and conditioning cycle are interrupted.
- Analog output transmission is stopped, and the AOUT output pin is set to the idle state or active high (UDR) or low (LDR) as described in Table 3.2.
- OWI interface for one-wire communication is enabled. Both RAM output pages are readable. The *StrtCmdMd* command must be sent to switch to the Command Mode for further command processing.

- The ZSSC4151 can be restarted by the power-off/power-on sequence
- Some of the failure reactions set the output to either LDR or UDR. In this case, it is possible to select UDR or LDR via the NVM register $01_{HEX,}$ bit 13. This setting is valid for all failsafe tasks. Static DM is caused in most cases by ZSSC4151 hardware monitoring tasks, and these tasks cannot be disabled.

Table 3.2 Overview of Detected Failures for Static DM

	Failsafe Task	Description	Messaging Time	Failure Reaction
	Oscillator Fail	Detects faulty oscillator operation	< 200µs	Temporary DM (LDR)
Firmware Errors	Internal Error	Reading of ADC data was aborted	< FMT (see section 3.1.4.3)	LDR or UDR [a]
	NVM Invalid	Non-programmed NVM	Start-up	LDR
	Startup Phase	Sequence during startup violated	Start-up	Tri-state
Hardware Errors	RDAC Decoder Error	Read back of analog voltage from AOUT failed	< FMT	LDR or UDR [a]
	Broken-Chip Check Error	Detects a broken bare die device	< FMT	LDR or UDR [a]
	Configuration Error	CRC polynomial failure for NVM or ROM	Start-up	LDR or UDR [a]
	RAM Access Error	Access contention for RAM	< 200µs	LDR or UDR [a]
	RAM DMA Error	Access to wrong internal address	< 200µs	LDR or UDR [a]
	CMC APB Slave Error	Access failure on Advanced Peripheral Bus (APB) for CMC or any connected slave	< 200µs	LDR or UDR [a]
	Conditioning CRC Error	CRC polynomial failure for conditioning formula or measurement cycle.	< FMT	LDR or UDR [a]
	Measurement CRC Error			
	RAM CRC Error	CRC polynomial failure for RAM	< FMT	LDR or UDR [a]
	RAM Parity Error	Parity check ensuring data content of RAM	< FMT	LDR or UDR [a]
	CMC Error	ROM CRC incorrect or program memory access or interrupt overflow error	< FMT	LDR or UDR [a]
	Watchdog Timeout	Detection of watchdog timeout for the start routine or measurement cycle No watchdog reset signal to the CMC.	Watchdog timeout 500ms delayed after the Static DM is entered.	LDR or UDR [a]

[a] The diagnostic range can be defined in the NVM. The default IDT delivery form will be set to the UDR.

3.1.4.2 Temporary Diagnostic Mode

In parallel to all hardware and firmware monitors, there are application monitors that will cause the Temporary Diagnostic Mode. Temporary events cause the output to be set to LDR or UDR as defined by configuration. If the failure event is no longer detected, the ZSSC4151 goes back to the normal output range.

If the Temporary Diagnostic Mode is activated, operation is affected as follows:

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering.
- Analog output transmission is continued indicating DM.
- The ZSSC4151 returns to NOM including analog output transmission of the valid sensor signal if fault checks do not detect further faults.

Note that the error detection functionality can be partly enabled or disabled by configuration words (e.g., sensor connection check, sensor aging (CMV) limits, ROM check, etc.).

For a list of available application monitors that can cause the Temporary Diagnostic Mode and their handling, refer to the *ZSSC4151 Application Description.*

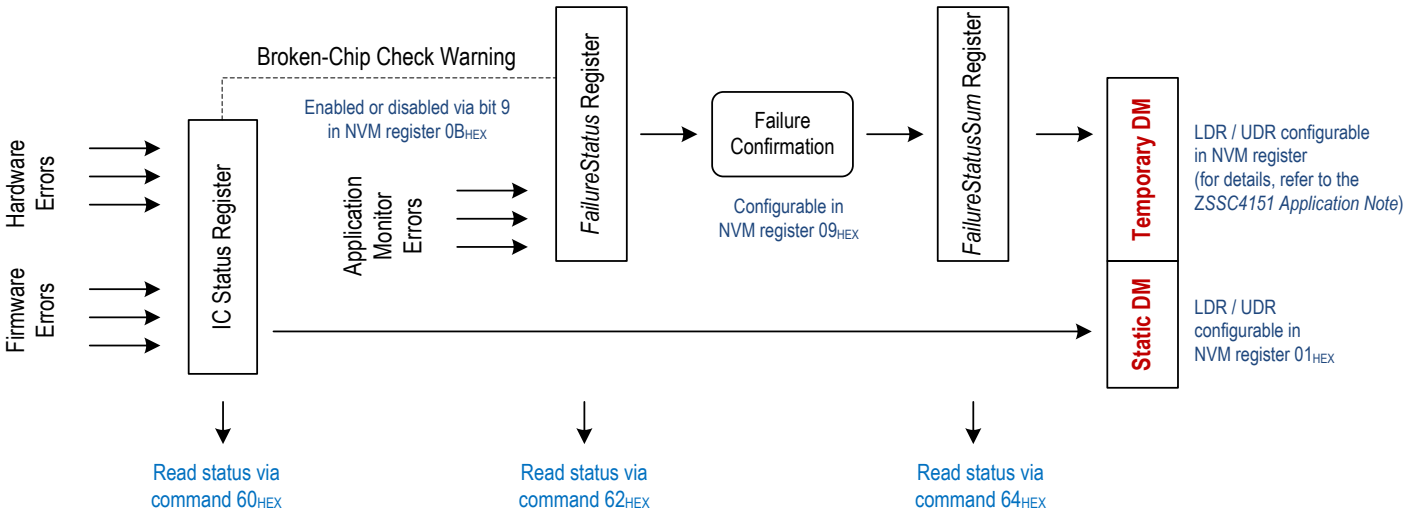
3.1.4.3 Failure Confirmation and Diagnostic Mode Generation

In the event that an application monitor triggers a failure event, it will be reported in the ZSSC4151 internal *FailureStatus* register. Reading this register is possible with the *RdFailureStatus* command (62_{HEX}). The failure event will be re-checked once in every complete measurement and conditioning cycle. If the failure is confirmed, it will be transferred to the *FailureStatusSum* register. This can be read via the command *RdFailureStatusSum* (64_{HEX}). Both commands are described in the *ZSSC4151 Commands* document. Failure confirmation is configurable in NVM allowing selection of either a fast failure messaging time (FMT) or a more robust application setup.

In the event that a hardware or firmware failure is triggered this will not be confirmed and instead the failure is directly reported via the Static Diagnostic Mode.

Figure 3.2 illustrates the signal flow from the hardware, firmware, and application monitors to either the Static or Temporary Diagnostic Mode.

Figure 3.2 Process Flow for Failure Confirmation



3.2 Failsafe Tasks for Temporary Diagnostic Mode

Various sources for failures will cause that the ZSSC4151 will go into Temporary Diagnostic Mode as described in the following sections. For further details on when these failsafe tasks are implemented and enabled/disabled, see the *ZSSC4151 Application Description*.

3.2.1 Power and Ground Loss

Power and ground loss cases are indicated by pulling the AOUT pin into the lower or upper diagnostic range (LDR/UDR) in the event of a lost node or load connection to ground or the supply. The ZSSC4151 is inactive in this case, and the specified leakage current in combination with the load resistor guarantees reaching the LDR or UDR.

3.2.2 AFE Gain Monitor

ZSSC4151 analog front end (AFE) provides an option to apply an input voltage by an internal AFE digital-to-analog converter (AFEDAC). Refer to Figure 2.1 for a detailed block diagram. This AFEDAC and its output voltage are used to monitor the correct function of the complete analog front end.

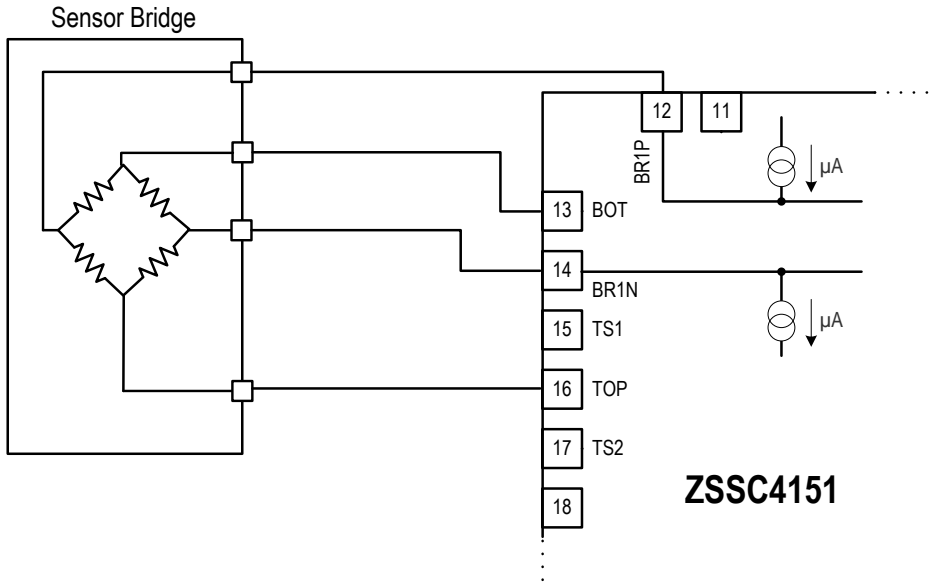
3.2.3 Sensor Check

The sensor check consists of two parts: the Sensor Connection Check (SCC) and Sensor Short Check (SSC). Both measurements will always be executed; however, evaluation of the test results can be enabled or disabled individually. Disabling is possible by setting the limits for the test functions to the minimum (8000_{HEX}) and maximum ($7FFF_{HEX}$) thresholds. Since disabling the actual measurements is not possible, disabling the monitoring limits will have no impact on the response time of the system.

The Sensor Connection Check will check if one of the four connection wires of the sensor bridge is broken. This option enables additional comparators that will monitor both differential inputs of the sensor bridge.

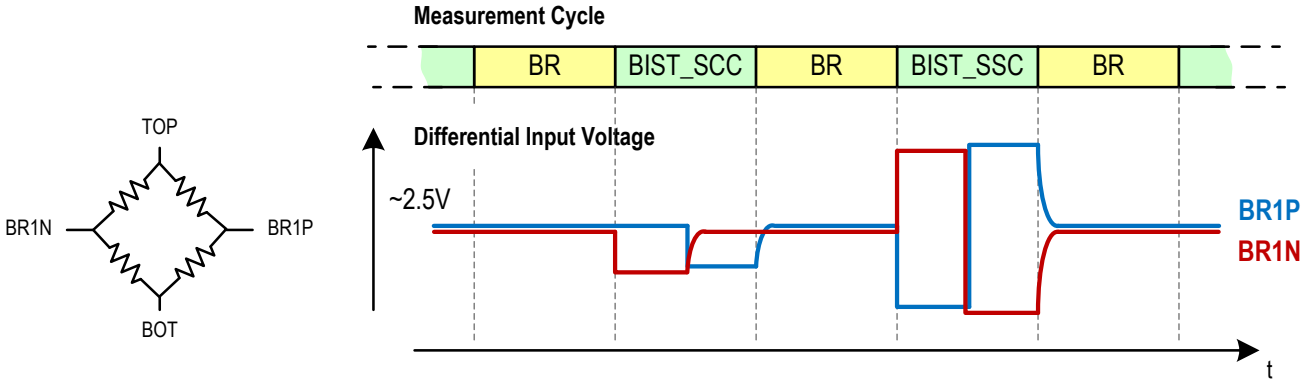
Figure 3.4 illustrates the principle of the Sensor Short Check. BOT and TOP will still be connected internally during this test.

Figure 3.3 Principle Schematic for the Sensor Bridge Short Check



Two measurement tasks are assigned for the sensor short detection. In order to avoid misinterpretations during both measurements, which could be caused by the voltage difference of the sensor bridge inputs, the SSC measurement is repeated with same current level but with a reverse polarity. Therefore there is an SSC+ and SSC- measurement running internally, which will only invert the current polarity on the bridge input pins. Figure 3.4 illustrates the sequence for the sensor short check measurement. During each measurement a small current is forced into the bridge by internal current sources. The voltage difference between BR1N and BR1P is measured as during a normal bridge conversion. If the voltage difference between both measurements is too small, a shorted sensor is detected.

Figure 3.4 Principle Sequence for Sensor Bridge Checks



The Sensor Connection Check (SCC) will detects a disconnected BR1N, BR1P, TOP, or BOT pin. During the SCC measurement, two tests are performed. In both test sets, a small current is applied to either the BR1N or BR1P pin. In the event of the loss of any connection, the pin will be forced to either the TOP or BOT signal, which will be detected by this procedure.

3.2.4 Sensor Common Mode Check

The ZSSC4151 offers another special method for sensor monitoring using the mean (common mode) voltage at the BR1P and BR1N pins. Typically both voltages are in the range of roughly 2.5V. A change in this voltage can indicate a change in the bridge sensor element. This can be caused by damage due to over-pressure events or aging of the sensor cells.

For this Common Mode Voltage (CMV) Check, two measurements are performed: one for each single bridge input (BR1P or BR1N) against a fixed internal reference voltage. These are measurement tasks 6 and 7, which are described in the *ZSSC4151 Application Description*. The difference between the two measurement results is calculated and the results are divided by, so the internal reference voltage will be eliminated.

$$Z_{CMV\_1} = \left(\frac{gain * \left(\left(V_{51.6\% \text{ of } V_{TOP\_BOT}} - V_{BR1P} \right) + V_{OFFSET} \right)}{ADC_{REF}} + rngsh \right) * 2^{15} \qquad \textbf{Equation 2}$$

$$Z_{CMV\_2} = \left(\frac{gain * \left(\left(V_{BR1N} - V_{51.6\% \text{ of } V_{TOP\_BOT}} \right) + V_{OFFSET} \right)}{ADC_{REF}} + rngsh \right) * 2^{15} \qquad \textbf{Equation 3}$$

Where

Z_{CMV_x}	Output counts of ADC for Common Mode of BR1P or BR1N
V_{TOP_BOT}	Bridge supply voltage (between TOP and BOT pins)
V_{OFFSET}	AFE offset voltage
gain	AFE gain: 1 to 200 (default: 2.1)
ADC_{REF}	ADC reference voltage between TOP and BOT pin
rngsh	ADC range shift: 0.5

Both individual measurement results will be combined in one single CMV result as specified in Equation 5. This result can be read from output memory address 19_{HEX} and will be monitored with limits stored in NVM addresses 34_{HEX} (lower limit) and 35_{HEX} (upper limit). These limits for the CMV check are defined during the calibration process for this function.

$$Z_{CORR\_CMV} = \frac{Z_{CMV\_1} - Z_{CMV\_2}}{2}$$ **Equation 4**

$$Z_{CORR\_CMV} = \left(\frac{gain * \left(2 * V_{51.6\% \text{ of } V_{TOP\_BOT}} - V_{BR1P} - V_{BR1N} \right)}{ADC_{REF}} \right) * 2^{14}$$ **Equation 5**

Depending on the sensing element and its characteristic changes over input stimuli data (e.g., pressure and temperature), the resistance ratio can change, and therefore the value for Z_{CORR_CMV} can also change. In other cases, Z_{CORR_CMV} might stay constant over input stimuli data.

Equation 5 shows the complete result of Equation 4. Since V_{BR1P} and V_{BR1N} result from the ratio of the external resistance connected to the TOP and BOT supply voltages, the result of Z_{CORR_CMV} will be a ratiometric measurement as well. A result of zero counts output for Z_{CORR_CMV} will be achieved when V_{BR1P} and V_{BR1N} are equal to 51.6% of the bridge supply, which is slightly more than 50% due to the internal DAC in the AFE. This has no effect on the basic function of the common mode voltage monitor.

The default gain setting for the ZSSC4151 is 2.1, and the default limits are $F000_{HEX}$ and 1000_{HEX}. This represents -4096_{DEC} and 4096_{DEC} counts since the limits will always be stored as signed integer data. Each count of Z_{CORR_CMV} is due to a change in the common mode voltage of 14.53ppm of V_{TOP_BOT}. Thus the limits will represent 45.65% to 57.55% of the bridge supply or 2.28V to 2.87V for a 5V bridge supply.

Example for a bridge supply voltage of 5.0V: One count of Z_{CORR_CMV} represents a 14.53ppm voltage change, which is 0.07265mV. For this example, $\pm 1000_{HEX}$ counts is equivalent to 297.57mV.

Calibration of the CMV monitor can be done in parallel during the calibration process for the input stimuli (e.g. pressure). Alternatively, theoretical limits can be calculated or determined during sensor module evaluation and permanently programmed for any calibrated sensor module. Using the calibration method requires acquiring the Z_{CORR_CMV} value at least twice and using a linear regression to calculate the minimum and maximum values for the application. With a proper margin (e.g., 3%), the lower and upper limits can be calculated and programmed individually for each sensor module.

Example: Calibration points were selected at 20% and 80% of the input stimuli value, and the end application will run from 5% to 95%. At each calibration point, Z_{CORR_CMV} was acquired with -100_{DEC} and 300_{DEC} counts. The margin for the CMV limits is set to 1%, which can cover effects such as temperature and limited aging of the sensing element.

With acquired Z_{CORR_CMV} raw data, the minimum and maximum data for the application will result in -200 and 400 counts. A 1% margin based on a data input range of 2^{15} leads to a deviation of 328 counts. Thus the limits should be set to $-528_{DEC} = FDF0_{HEX}$ and $728_{DEC} = 2D8_{HEX}$.

3.3 Measurement and Conditioning Cycle

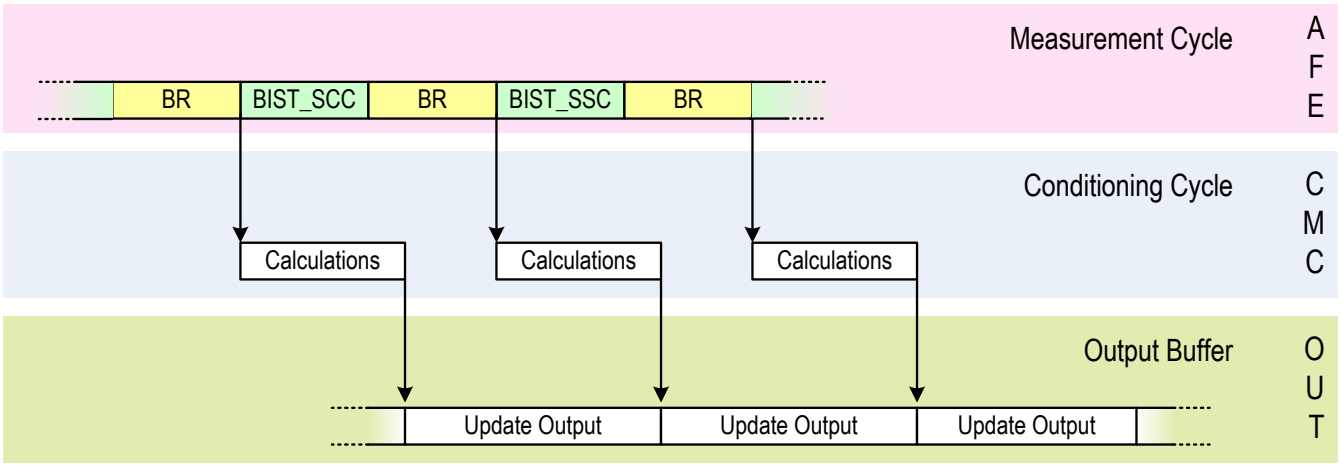
3.3.1 General

During Normal Operation Mode, the ZSSC4151 will start the configured measurement cycle. In parallel, the conditioning cycle will be started. Both cycles will be synchronized. The measurement cycle defines a list of measurements that will be performed in a sequence. The list of measurements depends on the configuration as described in the *ZSSC4151 Application Description*. Control of the AFE internal multiplexer is done by the CMC. After power-on, there is a special startup routine that will perform measurements that are required for the first valid bridge output data as described in the *ZSSC4151 Application Description*.

As soon as a new bridge measurement result is available, a new conditioning cycle will be started. The conditioning cycle defines single calculation steps that are performed by CMC. As a result, new compensated bridge output data is available that will be transferred to the output buffer.

Figure 3.5 illustrates the structure of the measurement and conditioning cycle.

Figure 3.5 Principle Measurement and Conditioning Cycle



4. Serial Digital Interfaces

4.1 General

The ZSSC4151 includes a serial digital interface (SIF), which is able to interact using two communication protocols: I2C and the ZACwire™ one-wire interface (OWI). The SIF enables programming of the ZSSC4151 to configure its application mode and to calibrate its conditioning equations. The SIF provides the readout of the conditioned result of the measured value as a digital value. The ZSSC4151 always operates as a slave.

The communication protocol is selectable. In Command Mode (CM) both I2C and OWI communication protocols are available. In Normal Operating Mode (NOM), the conditioned results are continuously updated and available to be read as an analog output from AOUT. The access mode for OWI communication is programmable (see section 4.3 for details).

A command consists of a device address, a READ/WRITE bit, and a command byte. Some commands (e.g., writing data into the ZSSC4151) also involve additional data bytes; this is independent of the communication protocol used. Refer to the *ZSSC4151 Commands* for detailed information about command setup.

There are two general types of requests used to read data via the SIF from the ZSSC4151:

- Continuously reading the conditioned result in NOM – analog out
- Reading of internal data, e.g. RAM or nonvolatile memory (NVM) content, or acquired measurement data in CM for calibration and/or configuration tasks

To read internal and/or measurement data in CM from the ZSSC4151, normally a specific command must be sent to transfer this data into the output registers of the SIF. Thereafter a READ command is used to retrieve this data. The data transmission is repeated until the master sends a stop condition. This is independent of the communication protocol used.

4.1.1 Addressing

Addressing is supported by the I2C and ZACwire™ (OWI) interface. Every slave connected to the master responds to a specific address. After generating the start condition, the master sends the address byte containing a 7-bit address followed by a data direction bit (READ/WRITE). A '0' indicates a transmission from master to slave (WRITE); a '1' indicates a data request (READ).

The general ZSSC4151 slave address is 28_{HEX} (7-bit). When using I2C, the addressed slave answers with an acknowledge while all other slaves connected to the master normally ignore this communication. Via ZSSC4151 programming, it is possible to allocate and activate an additional available slave address. In this case, the device recognizes communication on both addresses, on the general one and on the additional one. The slave addresses can be configured with NVM register 01_{HEX} as defined in Table 4.1.

Table 4.1 OWI and I2C Addressing

Bits [15:14] of NVM Register 01_{HEX}	Definition	Description
00_{BIN}	28_{HEX}	ZSSC4151 can be addressed via 28_{HEX} address only.
01_{BIN}	29_{HEX}	ZSSC4151 can be addressed via 28_{HEX} and 29_{HEX} addresses.
10_{BIN}	$2A_{HEX}$	ZSSC4151 can be addressed via 28_{HEX} and $2A_{HEX}$ addresses.
11_{BIN}	$2B_{HEX}$	ZSSC4151 can be addressed via 28_{HEX} and $2B_{HEX}$ addresses.

4.1.2 Communication Verification

A READ request received by a ZSSC4151 is answered with the command that is being answered and data present in the SIF output registers (typically 2 bytes). If the command that was sent to the ZSSC4151 is not a valid command the answer will contain an error indication inside the command response as described in Table 4.2. Details of available commands are provided in *ZSSC4151 Commands*.

Table 4.2 Command Response Format

Command	Command Response Byte								Data Words
	7	6	5	4	3	2	1	0	
Command in execution, response pending	0	0	0	0	0	0	0	0	–
Command successfully processed	0	7-Bit Command							[Return Data]
Reserved	0	1	1	1	1	1	1	1	–
Command unknown	1	0	0	0	0	0	0	0	80_{HEX} General Rejection
Command rejected	1	7-Bit Command							80_{HEX} General Rejection
Mandatory data not in range	1	7-Bit Command							40_{HEX} Argument Error
Command not authorized	1	7-Bit Command							20_{HEX} Not Authorized
Command request byte aborted	1	7-Bit Command							10_{HEX} Incomplete
Mandatory data aborted									
Mandatory data CRC aborted									

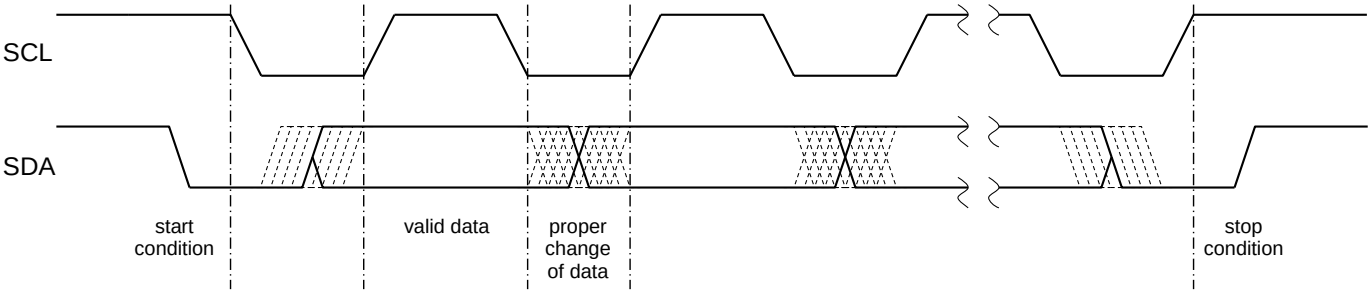
1.1.1. Communication Protocol Selection

Both I2C and OWI protocols are active in parallel, but only one interface can be used at a time.

4.2 I2C Protocol

For I2C communication, a data line (SDA) and a clock line (SCL) are required.

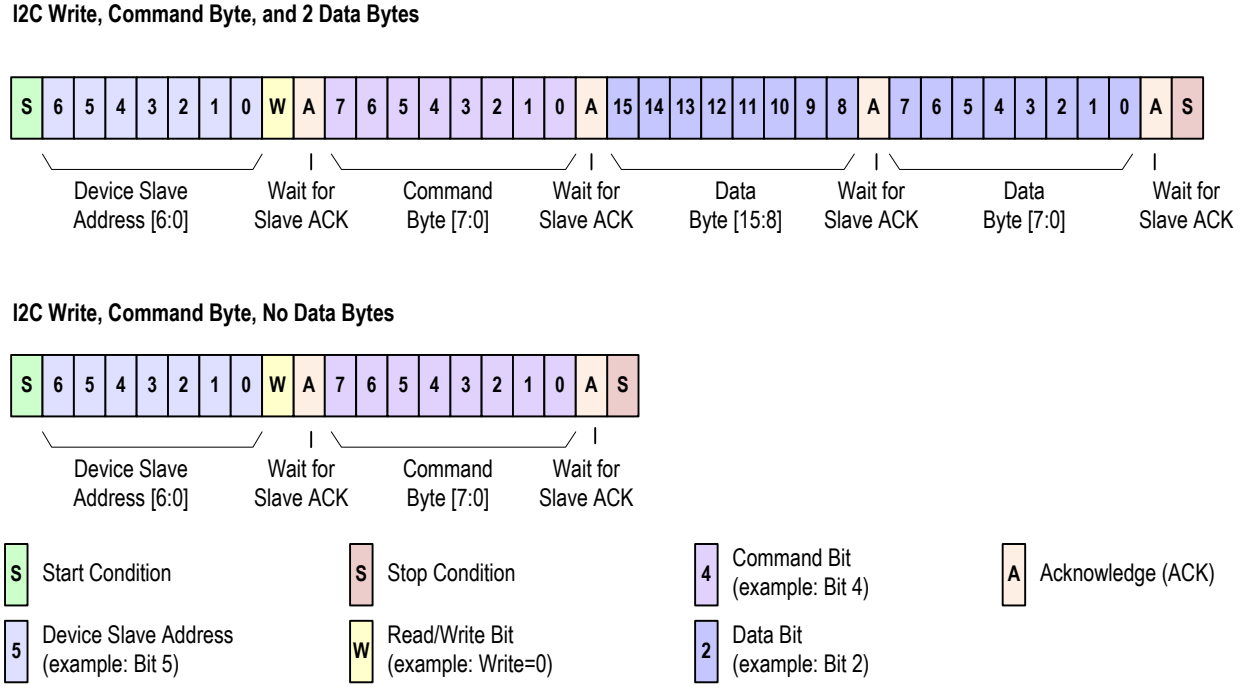
Figure 4.1 I2C – Principles of I2C Protocol



The I2C communication and protocol used is defined as follows:

- **Idle Period**
  During inactivity of the bus, SDA and SCL are pulled-up to the supply voltage VDDA by R_{I2C_PULLUP}.
- **Start Condition**
  A high-to-low transition on SDA while SCL is at the high level indicates a start condition. Every command must be initiated by a start condition sent by a master.
- **Stop Condition**
  A low-to-high transition on SDA while SCL is at the high level indicates a stop condition. A command must be closed by a stop condition to start processing the command routine in the ZSSC4151.
- **Valid Data**
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Each byte transmitted is followed by an acknowledge bit. Transmitted bits are valid if, after a start condition, SDA remains at a constant level during the high period of SCL. The SDA level may change only when the clock signal at SCL is low.
- **Acknowledge**
  An acknowledge after a transmitted byte is obligatory. The master must generate an acknowledge-related clock pulse. The receiver (slave or master) pulls down the SDA line during the acknowledge clock pulse. If no acknowledge is generated by the receiver, a transmitting slave will become inactive. A transmitting master can abort the transmission by generating a stop condition and can repeat the command. A receiving master may signal the end of the transfer to the transmitting slave by not generating an acknowledge-related clock pulse at SCL. The ZSSC4151 changes to inactive interface mode when processing internal command routines started by a previously sent command.
- **WRITE Operation**
  An I2C WRITE operation is initiated by the master sending the slave an address byte including a data direction bit set to '0' (WRITE). The address byte is followed by a command byte, and for applicable commands, additional data bytes (optional). The ZSSC4151 internal microcontroller evaluates the received command and processes the related routine. Figure 4.2 illustrates a WRITE command with two data bytes and another WRITE command without data bytes. A detailed description of the command set is given in *ZSSC4151 Commands*.

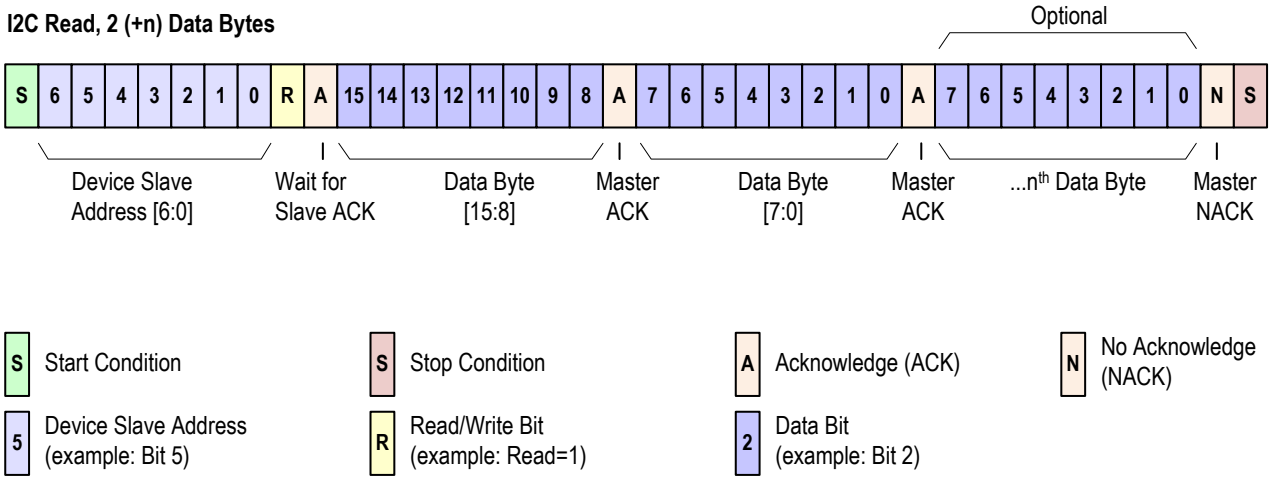
Figure 4.2 I2C – Write Operation (e.g. Sending 2 Data Bytes)



- **READ Operation**
  A data request from a master to a slave is initiated by sending an address byte including a data direction bit set to '1' (READ). The slave answers by sending data from the interface output registers. The master must generate the transmission clock for the following: SCL, acknowledges after each data byte (except after the last one), and the stop condition at the end. A data request is handled by the ZSSC4151's interface module and consequently does not interrupt the current process of the internal microcontroller.

  Note: The data in the activated registers is sent continuously until a stop condition is detected; after transmitting all available data, the slave starts repeating the data.

Figure 4.3 I2C – Read Operation – Data Request



A READ operation does not interrupt the current process of the internal calibration microcontroller and consequently an active and running measurement cycle will not be aborted. This allows continuously reading of data.

Figure 4.4 I2C – Timing Protocol

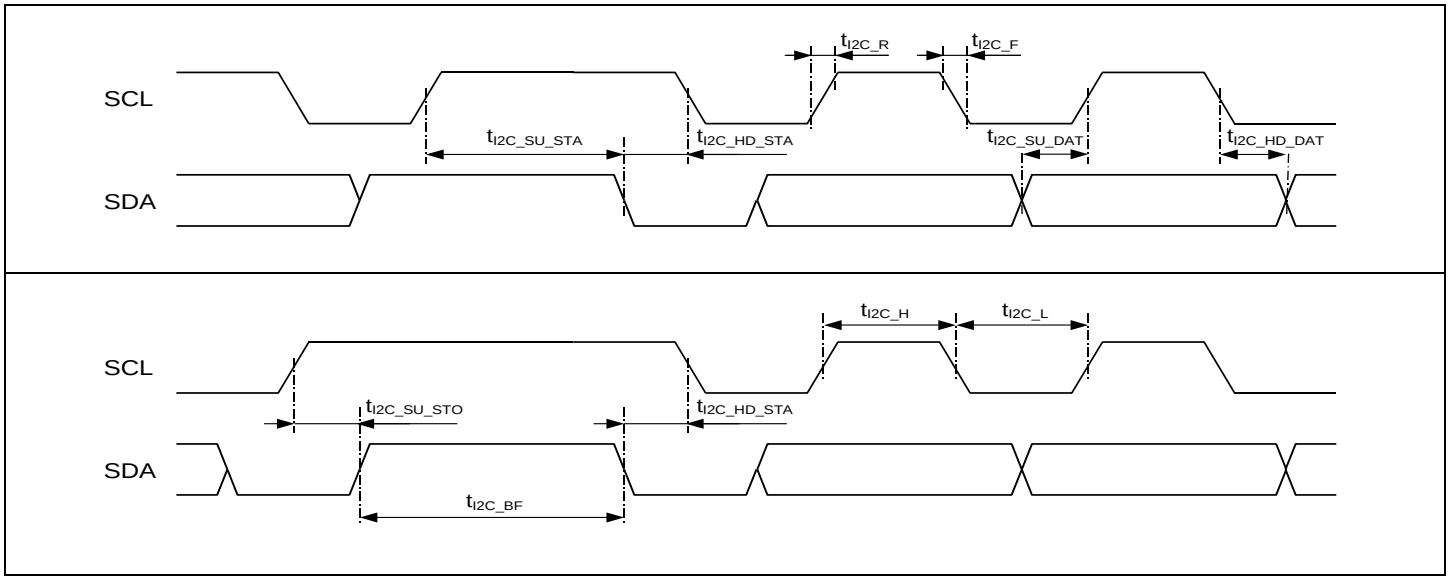


Table 4.3 Timing I2C Protocol

Nr.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1	SCL clock frequency	f_{SCL}				400	kHz
2	Bus free time between start and stop condition	t_{I2C_BF}		1.3			µs
3	Hold time start condition	$t_{I2C\_HD\_STA}$		0.6			µs
4	Setup time repeated start condition	$t_{I2C\_SU\_STA}$		0.6			µs
5	Low period SCL/SDA	t_{I2C_L}		1.3			µs
6	High period SCL/SDA	t_{I2C_H}		0.6			µs
7	Data hold time	$t_{I2C\_HD\_DAT}$		0			µs
8	Data setup time	$t_{I2C\_SU\_DAT}$		0.1			µs
9	Rise time SCL/SDA	t_{I2C_R}				0.3	µs
10	Fall time SCL/SDA	t_{I2C_F}				0.3	µs
11	Setup time stop condition	$t_{I2C\_SU\_STO}$		0.6			µs
12	Noise interception SDA/SCL	t_{I2C_NI}	Spike suppression			50	ns

4.3 Digital One-Wire Interface (OWI)

The ZSSC4151 implements IDT's ZACwire™ interface, a digital one-wire interface (OWI). It combines a simple and easy protocol adaptation with a cost-saving pin sharing. The communication principle of the OWI interface is derived from the I2C protocol. Becoming familiar with the I2C protocol is recommended to aid in understanding the OWI communication protocol. An advantage of OWI output signal capability is that it enables end-of-line calibration – no additional pins are required to digitally calibrate a finished assembly.

4.3.1 OWI Properties and Parameters

The ZSSC4151 functions as an OWI slave. An external master must control the communication by transmitting requests or reading responses. Figure 4.5 explains the basic principles of the physical OWI connection. Note that pulling up the OWI connection line must be done externally since the ZSSC4151 only has the capability to drive the OWI line active low.

OWI communication is self-locking (synchronizing) on the master's communication speed in the range of the defined OWI bit time.

Figure 4.5 Block Schematic of an OWI Connection

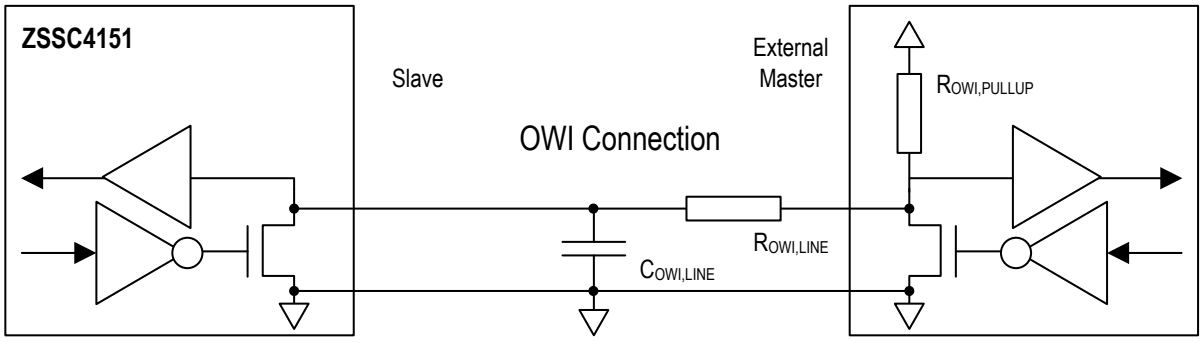


Table 4.4 OWI Interface Dimensioning

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1	Master pull-up resistance	$R_{OWI,PULLUP}$	0.47	1	10	kΩ	
2	OWI line resistance	$R_{OWI,LINE}$	0		47	Ω	$R_{OWI,LINE} < R_{OWI,PULLUP} / 100$
3	OWI load capacitance	$C_{OWI,LINE}$	4		150	nF	Total OWI line load including capacitive load inside the sensor module

4.4 OWI Protocol

The OWI protocol is defined as follows:

- **Idle Period**

  During inactivity of the bus, the OWI line is pulled up to supply voltage VDDE by an external resistor.

- **Start Condition**

  When the OWI line is in idle mode, a low pulse with a minimum $t_{OWI,START}$ width followed by a return to high indicates a start condition. Every request must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode so it is mandatory to bring OWI line to idle state for at least $t_{OWI,IDLE}$.

- **Valid Data**

  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, $t_{OWI,BIT}$ in Figure 4.6). A duty ratio greater than 1/8 and less than 3/8 is detected as '0', a duty ratio greater than 5/8 and less than 7/8 is detected as '1'. The bit period of consecutive bits must not increase to more than 1.5 times the previous bit period or decrease to less than half of the previous bit period because a stop condition is detected in this case.

  OWI protocol timing and parameters are specified in Figure 4.6 and in Table 4.5.

Figure 4.6 OWI Protocol Timing

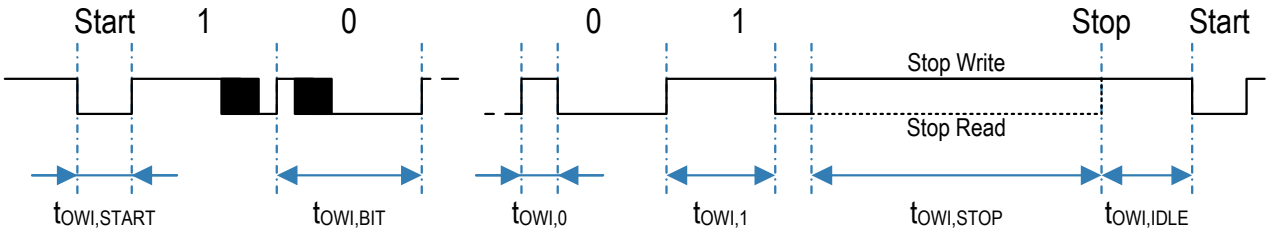


Table 4.5 OWI Protocol Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1	Bus free time	$t_{OWI,IDLE}$	25			µs	Between stop and start conditions
2	Hold time start condition	$t_{OWI,START}$	25			µs	
3	Bit time *	$t_{OWI,BIT}$	20		8000	µs	$t_{OWI,BIT} \geq 5 * R_{OWI,PULLUP} * C_{OWI,LINE}$

* Note that the achievable minimum bit time depends on the specific OWI line wiring according to Figure 4.5 and Table 4.4.

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
4	Duty ratio bit '0'	$t_{OWI,0}$	0.125	0.25	0.375	$t_{OWI,BIT}$	
5	Duty ratio bit '1'	$t_{OWI,1}$	0.625	0.75	0.875	$t_{OWI,BIT}$	
6	Hold time stop condition	$t_{OWI,STOP}$	2.0	3		$t_{OWI,BIT}$	Depends on the bit time of the last valid transmitted bit
7	Bit time deviation	$t_{OWI,BIT,DEV}$	0.55	1.0	1.5	$t_{OWI,BIT}$	Current bit time to previous bit time

- **Stop Condition**

  A constant level at the OWI line (no transition from low to high or from high to low) for at least twice the period of the last transmitted valid bit indicates a stop condition. Without considering the last bit-time, a stop condition is generated with a constant level at the OWI line for at least 30ms.

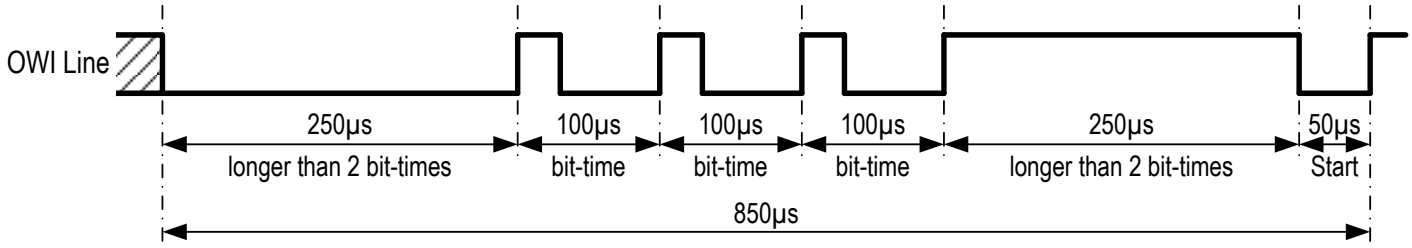
  The master finishes a request (transmission of a command to a slave) by returning to the high level (idle level) and then waiting the required time for the stop condition ($t_{OWI,STOP}$). A request (refer to the subsequent "Request Operation" section) must be closed by a stop condition to start the execution of the requested command.

  To interrupt a response while a slave is transmitting data to the master, the master must clamp the OWI line to the low level for generating a stop condition. Every response (refer to the subsequent "Response Operation" section) must be finished by a stop condition to stop the slave transmitting data.

  A stop condition is also detected if the bit-time of two consecutive bits increases to more than 1.5 times the previous bit period or decreases to less than half of the previous bit period. Additionally, a stop condition is detected if a bit-time shorter than 8µs or longer than 16.4ms is evaluated.

  To ensure correct communication, e.g. when analog output is running, the master should first generate a secured stop condition by sending a sequence as shown in Figure 4.7 before sending the 1st valid command to the ZSSC4151. These secure stop condition is recommended in all cases when master wants to force ZSSC4151 slave to listen to the next command.

Figure 4.7 Starting OWI Communication with a Secure Stop Condition

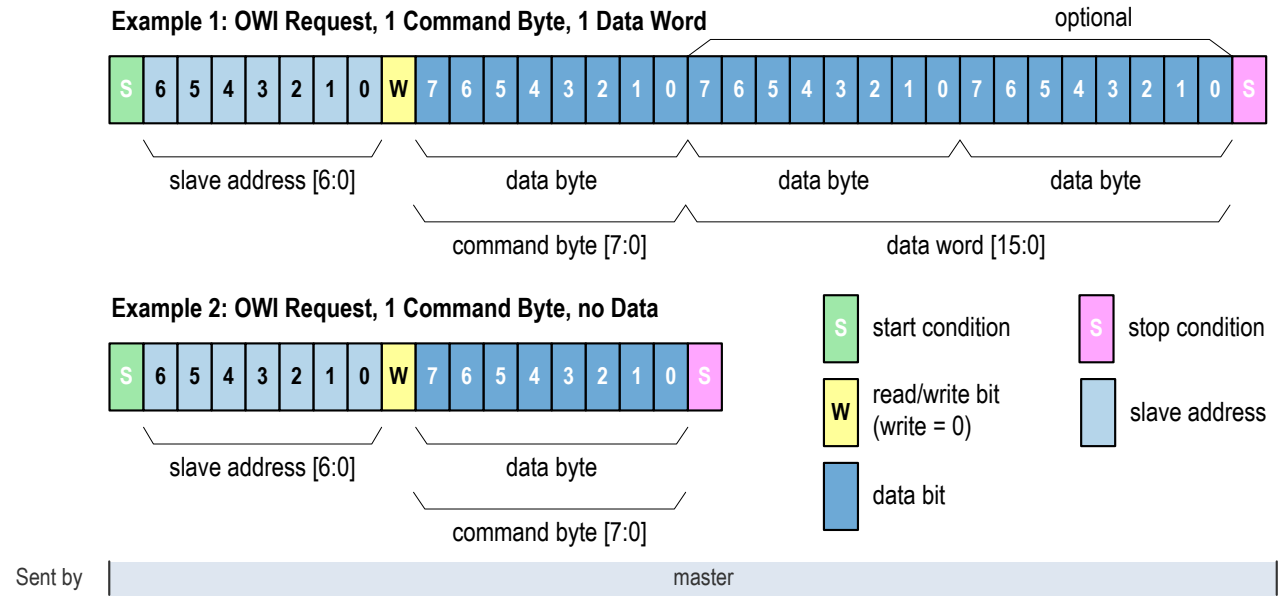


- **Request Operation**

  Request operations are transmitted from the master to a slave. Request operations consist of a start condition, a slave address, a READ/WRITE bit equal to 0 for a WRITE, a request command code with supporting information if necessary, and a stop condition. After receiving a valid request, the calibration microcontroller processes the requested routine. Figure 4.8 illustrates the transmission of a command with one data word and transmission of a command without data as examples for request operations. A description of the available command set is given in *ZSSC4151 Commands.*

  During WRITE operations only the OWI master will force the OWI communication line.

Figure 4.8 OWI Request Operation



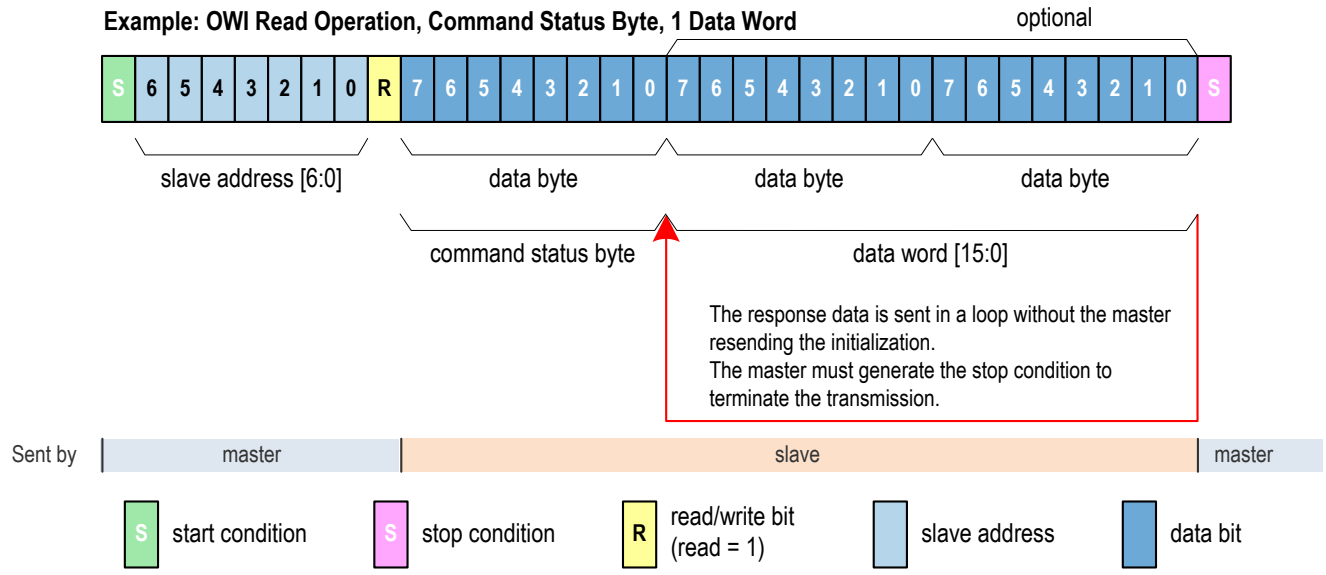
- **Response Operation**

  Response operations are initiated by the master by transmitting a start condition, a slave address, and a READ/WRITE bit equal to 1 for a READ. The slave answers by sending the response. The master must finish the communication by generating a stop condition. If the slave has sent the response without receiving a stop condition, it starts repeating the response data.

  The slave generates the data bits with a bit-time equal to the received READ/WRITE bit. It is possible to define a fixed bit-time for the response by using the command *WrOwiTxBitrate* as described in *ZSSC4151 Commands.*

  Figure 4.9 illustrates the transmission of a response with one data word as an example for a response operation. A description of the response data associated with the available commands is given in the *ZSSC4151 Commands.*

Figure 4.9 OWI Response Operation



5. Analog Output

5.1 Power-on Behavior

After power-on, the ZSSC4151 starts with a high-impedance output level at pin AOUT while processing the initialization and the configuration from NVM. Refer to section 3.1.2 for details on the startup routine. If no hardware failure is detected, a one-wire communication startup window after power-on allows starting the Command Mode by sending the command *StrtCmdMd*. This startup window is available in every output mode and is defined by parameter $t_{OWI\_STARTWIN}$ in the *ZSSC4151 Datasheet*. In the event of detection of a failure event as described in section 3.1.4.1, the ZSSC4151 will enter the Static Diagnostic Mode and report the failure.

Four different output modes are available that can be configured in the NVM register 01_{HEX} bits 4:3. For details for the complete NVM register 01_{HEX} refer *ZSSC4151 NVM Map*.

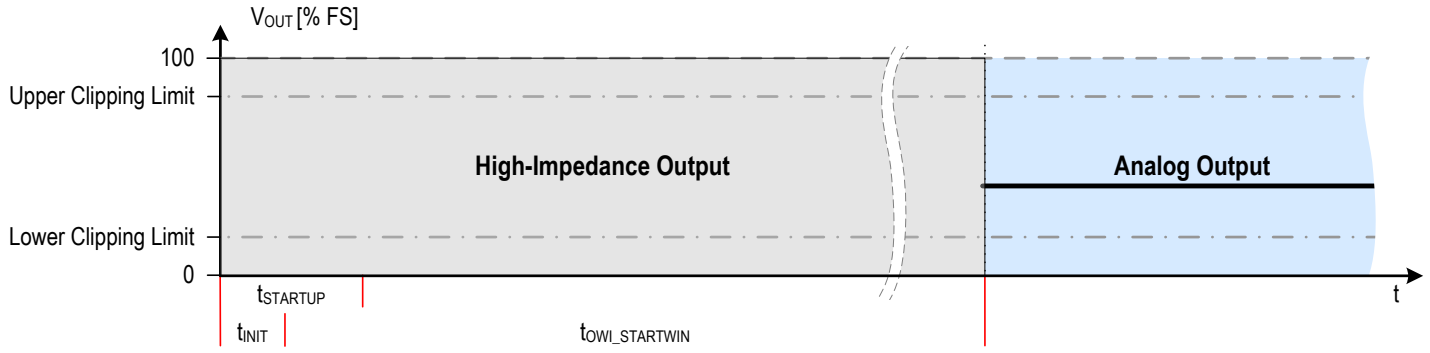
Table 5.1 Operation Modes for Analog Output Pin

NVM Register 01_{HEX} Bits [4:3]	Interpretation	Short Description
00_{BIN}	AOUT_CYC_WIN	Start AOUT transmission after first conditioning cycle and OWI start window
01_{BIN}	AOUT_CYC	Start AOUT transmission after first conditioning cycle with OWI start window in parallel
10_{BIN}	AOUT_WIN	Start AOUT transmission after OWI start window
11_{BIN}	OWI	OWI only; AOUT disabled

5.1.1 Start AOUT after First Conditioning Cycle and OWI Start Window (AOUT_CYC_WIN)

Upon delivery for the ZSSC4151, the default mode of the AOUT is AOUT_CYC_WIN since it facilitates configuration, calibration, and evaluation. In this mode, AOUT will stay in the tri-state condition during the complete OWI start-up window and if the initial measurement and conditioning cycle ($t_{STARTUP}$ – refer to section 3.1.2) has not finished within this timeframe, the ZSSC4151 will wait until the startup phase is completed. Figure 5.1 illustrates the power-on behavior for this configuration. This mode allows the communication master to use an open-drain output for communication purposes.

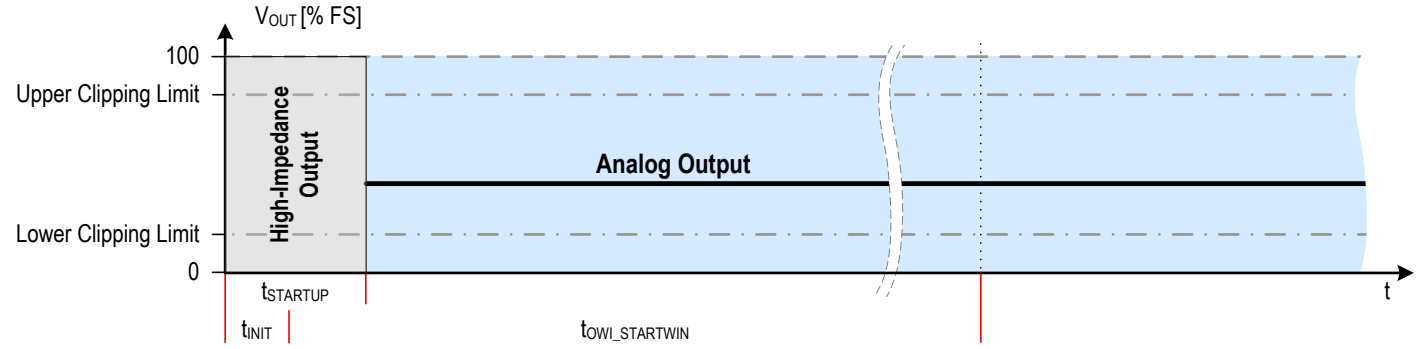
Figure 5.1 Power-on Behavior for the AOUT Analog Output after the OWI Start Window – AOUT_CYC_WIN



5.1.2 Start AOUT after the First Conditioning Cycle (AOUT_CYC)

The AOUT_CYC Mode provides the fastest power-up time for the ZSSC4151. In this mode, the analog output will be set to tri-state after power-on. In parallel, the internal measurement and conditioning cycle will be started. After the first valid bridge data and all necessary measurements such as temperature or auto-zero measurements are available, the analog output pin will be set to the new pressure data. Entering the Command Mode is still possible because the OWI start window takes place in parallel. In this mode, the OWI master must be able to overdrive the output buffer of the ZSSC4151 so that the ZSSC4151 will receive the start command mode command (*StrtCmdMd*).

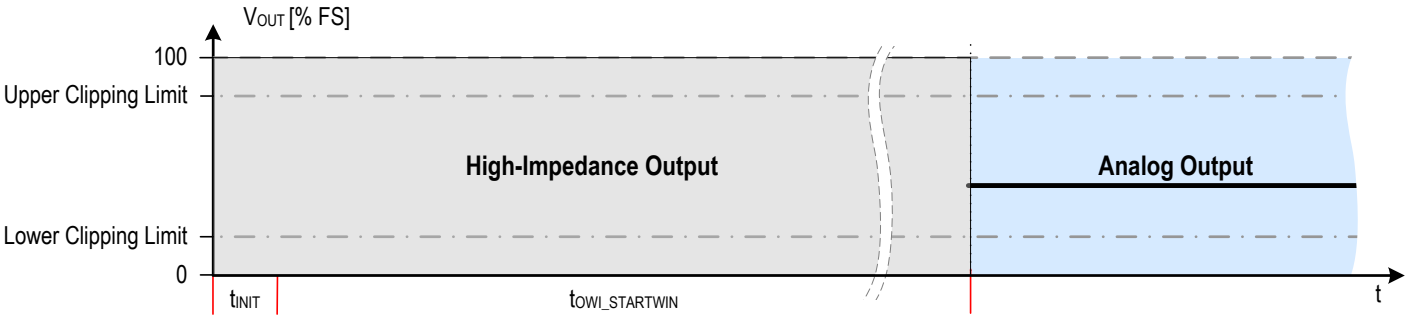
Figure 5.2 Power-on Behavior for Immediate Analog Output – AOUT_CYC



5.1.3 Start AOUT after OWI Start Window (AOUT_WIN)

The AOUT_WIN Mode functions the same as the AOUT_CYC_WIN Mode (see section 5.1.1) except that the startup phase is not applicable. In this mode, the analog output signal will always be active after finishing the OWI start window.

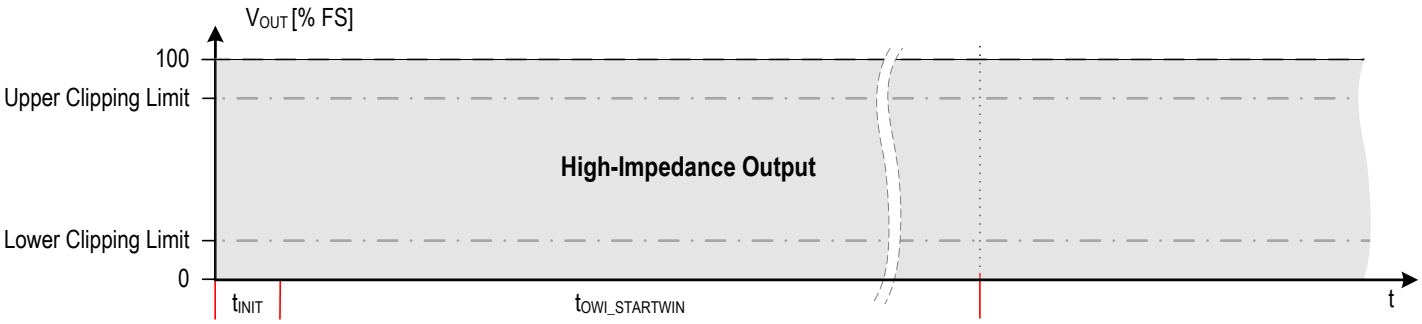
Figure 5.3 Power-on Behavior for the AOUT Analog Output after the OWI Start Window – AOUT_WIN



5.1.4 Start OWI Output Only (OWI)

In the OWI Mode, the analog output never starts. In this mode, the one-wire communication can be started using a standard open-drain master. The measurement and conditioning cycle runs immediately after the initialization. In OWI Mode, the startup window time limit is still active for starting the Command Mode if intended.

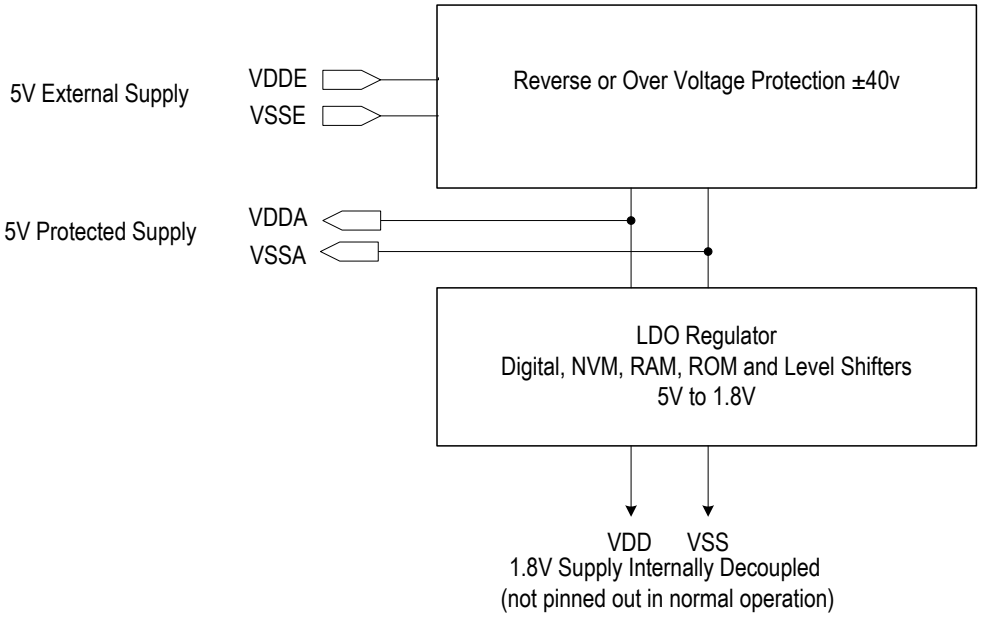
Figure 5.4 Power-on Behavior for OWI Mode (OWI)



6. Power Management

The power management for the ZSSC4151 is shown in Figure 6.1. The over-voltage/reverse-battery (OVRB) protection is a switch that opens if the external supply exceeds the normal operating voltage. The external supply pins are VDDE and VSSE. The protected 5V is VDDA and VSSA. These supply pins are protected from external OVRB and transients. VDDA and VSSA are used by the analog circuitry inside the ZSSC4151, and they supply the sensor bridge. Additionally, there is an internal low dropout (LDO) regulator that generates the digital supply of 1.8V. This regulator supplies the digital logic, memories (NVM, RAM, ROM), and level shifters. Decoupling capacitance for the regulator output is distributed over the digital block internally (no external component required). Refer to the *ZSSC415x Application Note – ZSSC4151 Power Management* for more details.

Figure 6.1 Power Management Overview



7. Glossary

Term	Description
APB	Advanced Peripheral Bus
ADC	Analog-to-Digital Converter
ALU	Arithmetic Logic Unit
AFE	Analog Front-End
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	(RAM) Direct Memory Access
DSP	Digital Signal Processor
FMT	Failure Messaging Time
GUI	Graphic User Interface
LDO	Low Dropout (Regulator)
LDR	Lower Diagnostic Range
LSB	Least Significant Bit
MSB	Most Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
NVM	Nonvolatile Memory
OVRB	Over-Voltage/Reverse-Battery
OWI	One-Wire Interface
PGA	Programmable Gain Amplifier
PTAT	Proportional to Absolute Temperature
RDAC	Resistive Digital-to-Analog Converter
RTD	Resistance Temperature Detector
SCC	Sensor Connection Check
SCCM	Sensor Check and Common Mode Adjustment Unit
SSC	Sensor Short Check or Sensor Signal Conditioner
UDR	Upper Diagnostic Range

8. Revision History

Revision Date	Description of Change
December 12, 2017	▪ AFE description extended (section 2). ▪ ADC description extended (section 2.4). ▪ CMC description added (Working Modes (section 3.1.1), Failsafe Tasks (section 3.2), and Measurement and Conditioning Cycle (section 3.3)). ▪ Added serial interface section (section 4) from a separate application note. That application note is now obsolete. ▪ Analog output description added (section 5). ▪ Added OWI and I2C section from a separate application note. ▪ Excluded TS2 for usage with external diode. ▪ The “Related Documents” section has been discontinued. Refer to the IDT product page for the current version of this document and the related documents: www.IDT.com/ZSSC4151. ▪ Minor edits.
February 8, 2016	Changed to IDT branding. Revision is now the release date.
September 3, 2015	First release.

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