

PMWD20XN

Dual N-channel μ TrenchMOS™ extremely low level FET

Rev. 02 — 26 April 2005

Product data sheet

1. Product profile

1.1 General description

Dual common drain N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Surface-mounted package
- Extremely low threshold voltage
- Low profile
- Fast switching

1.3 Applications

- Portable appliances
- Battery management

1.4 Quick reference data

- $V_{DS} \leq 20$ V
- $P_{tot} \leq 4.2$ W
- $I_D \leq 10.4$ A
- $R_{DSon} \leq 24$ m Ω

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 8	drain (D)	<p>SOT530-1 (TSSOP8)</p>	<p>mb1600</p>
2, 3	source1 (S1)		
4	gate1 (G1)		
5	gate2 (G2)		
6, 7	source2 (S2)		

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PMWD20XN	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1

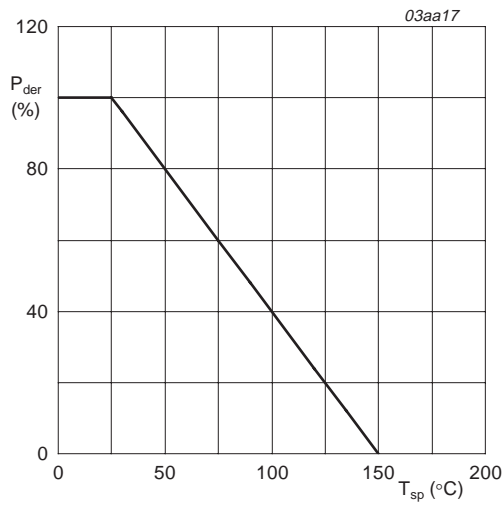
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

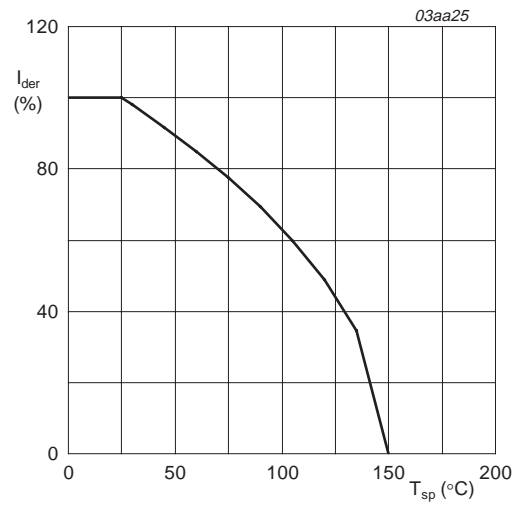
Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V	
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V	
V_{GS}	gate-source voltage (DC)		-	± 12	V	
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2 and 3	[1]	-	10.4	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2	[1]	-	6.5	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	[1]	-	41.7	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	[1]	-	4.2	W
T_{stg}	storage temperature		-55	+150	°C	
T_j	junction temperature		-55	+150	°C	
Source-drain diode						
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	[1]	-	3.5	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	[1]	-	14	A

[1] Single device conducting.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

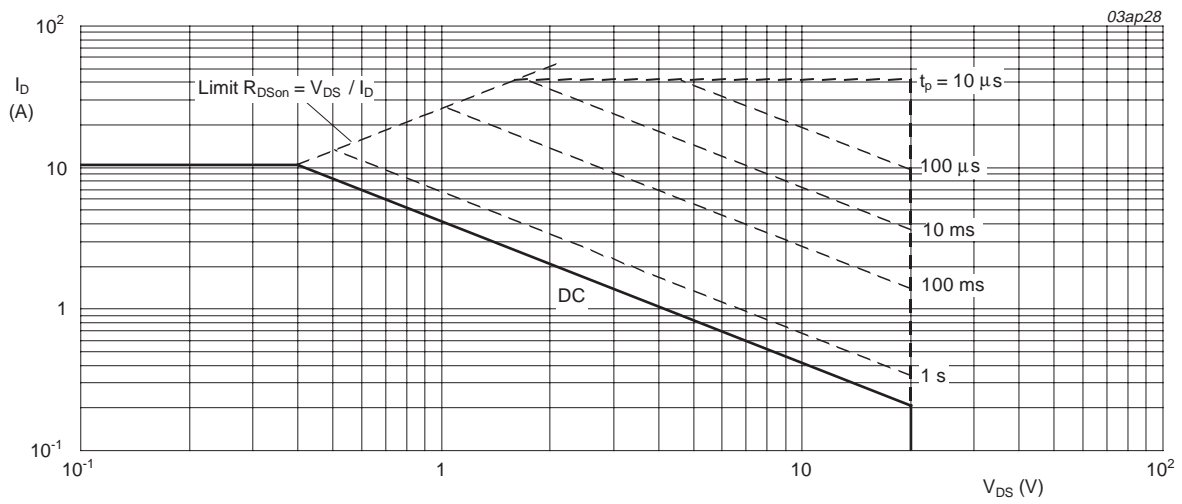
Fig 1. Normalized total power dissipation as a function of solder point temperature



$V_{GS} \geq 4.5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	30	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	100	-	K/W

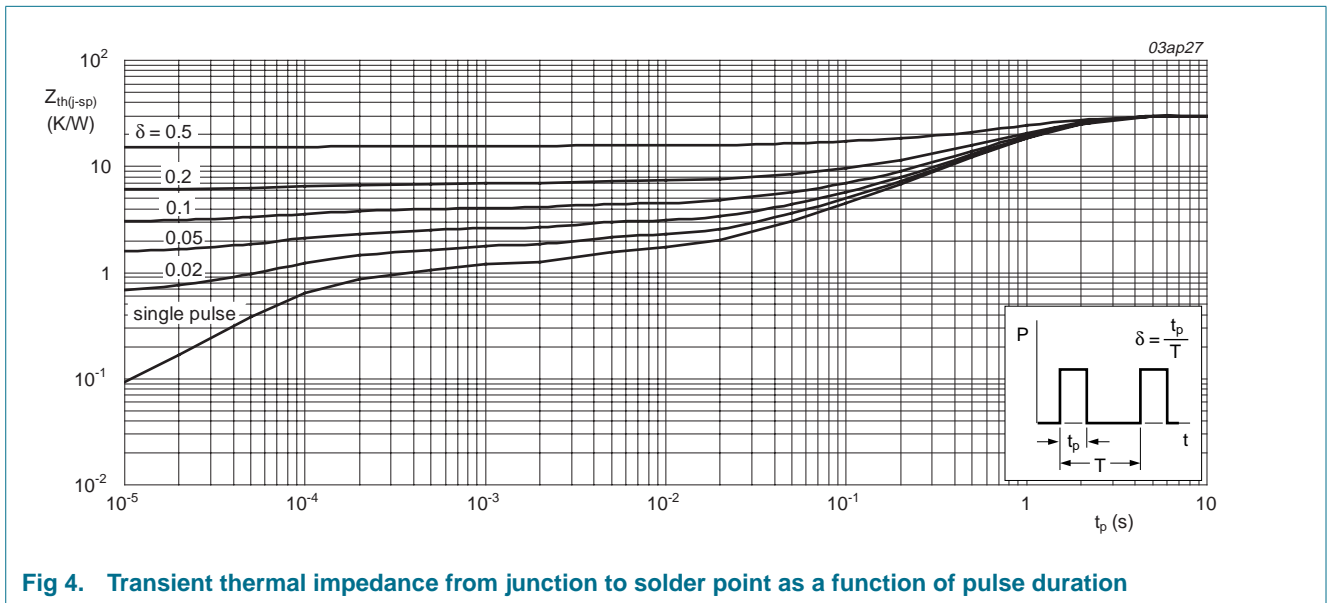
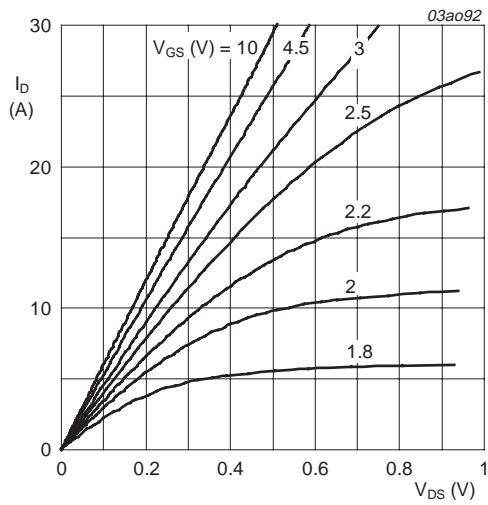


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

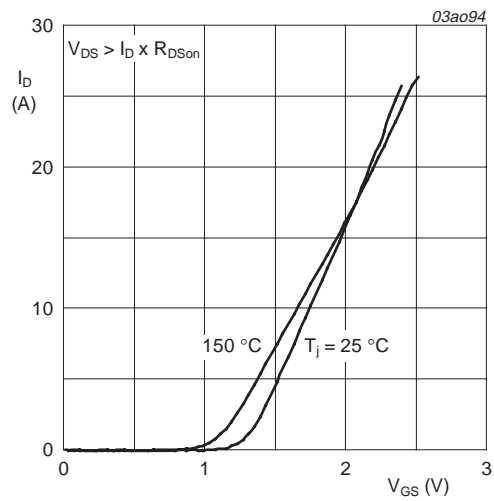
Table 5: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	20	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 and 10	0.5	-	1.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 12\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 4\text{ A}$; Figure 7 and 8 $T_j = 25\text{ }^\circ\text{C}$	-	20	24	m Ω
		$T_j = 150\text{ }^\circ\text{C}$	-	32	38.4	m Ω
		$V_{GS} = 2.5\text{ V}$; $I_D = 3\text{ A}$; Figure 7 and 8	-	27	34	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 4.2\text{ A}$; Figure 7 and 8	-	18	22	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 4\text{ A}$; $V_{DS} = 10\text{ V}$; $V_{GS} = 4.5\text{ V}$; Figure 13	-	11.6	-	nC
Q_{gs}	gate-source charge		-	1.8	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.7	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 16\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	740	-	pF
C_{oss}	output capacitance		-	200	-	pF
C_{rss}	reverse transfer capacitance		-	135	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10\text{ V}$; $R_L = 10\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	21	-	ns
t_r	rise time		-	31	-	ns
$t_{d(off)}$	turn-off delay time		-	44	-	ns
t_f	fall time		-	30	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 5\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.8	1.2	V



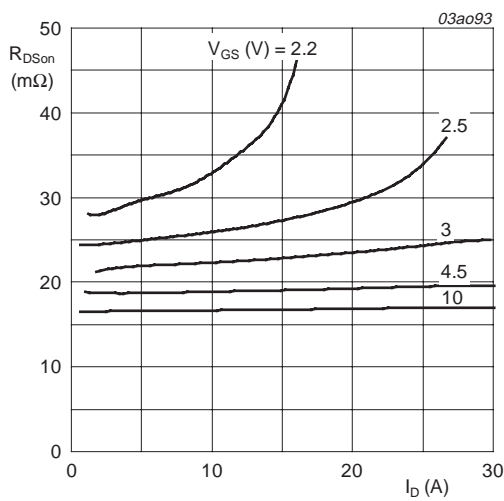
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



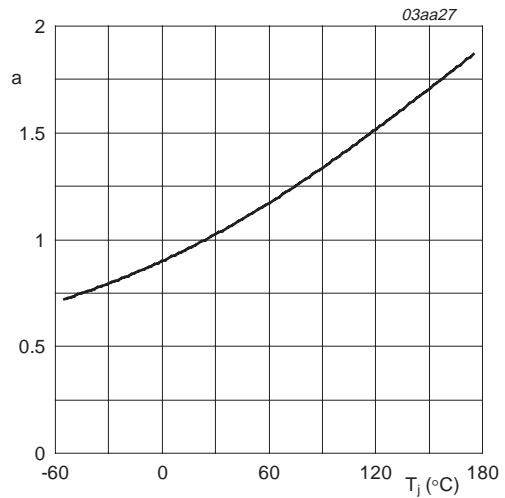
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



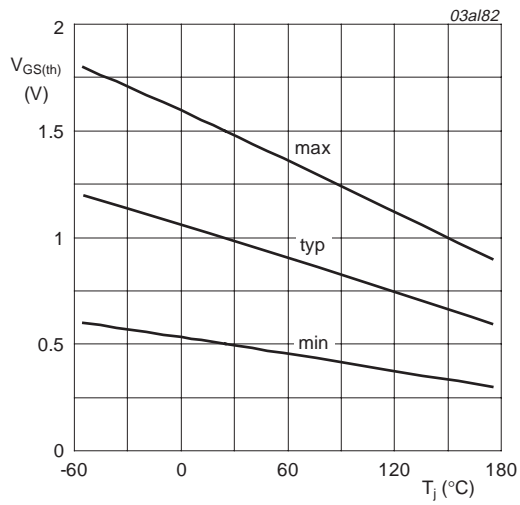
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



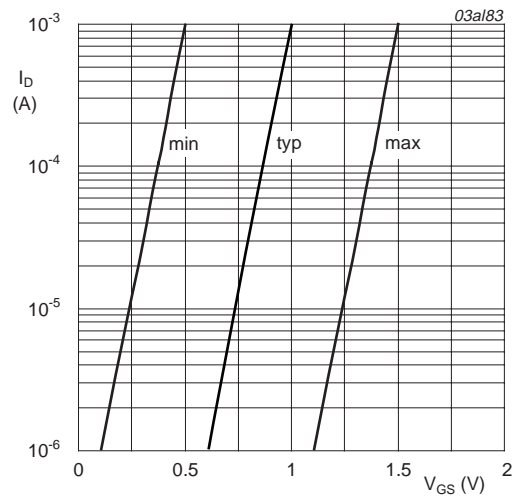
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



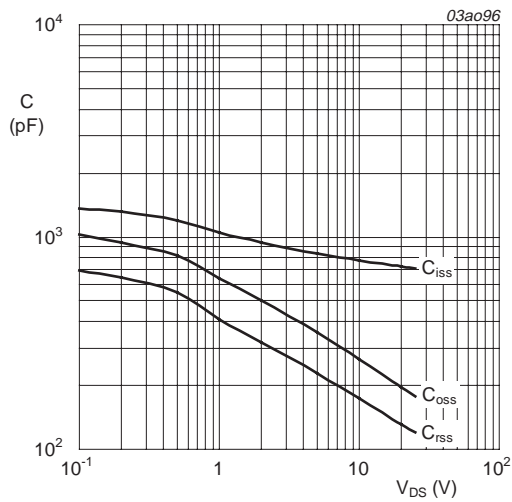
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



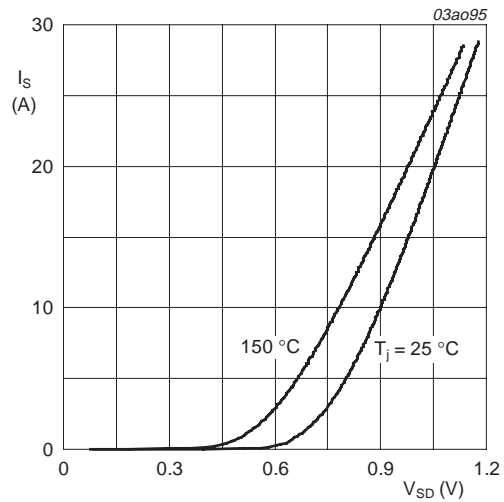
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



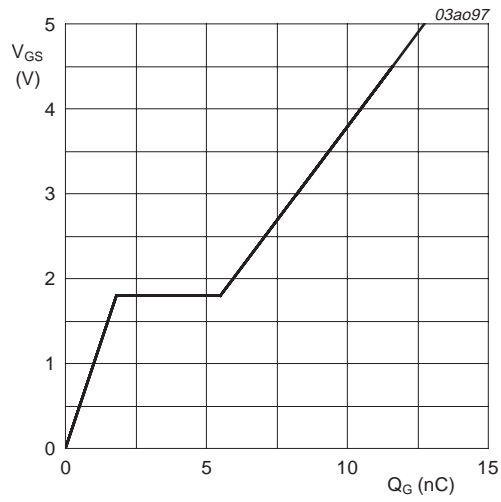
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25 \text{ }^\circ\text{C} \text{ and } 150 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



I_D = 4 A; V_{DD} = 10 V

Fig 13. Gate-source voltage as a function of gate charge; typical values

7. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm

SOT530-1

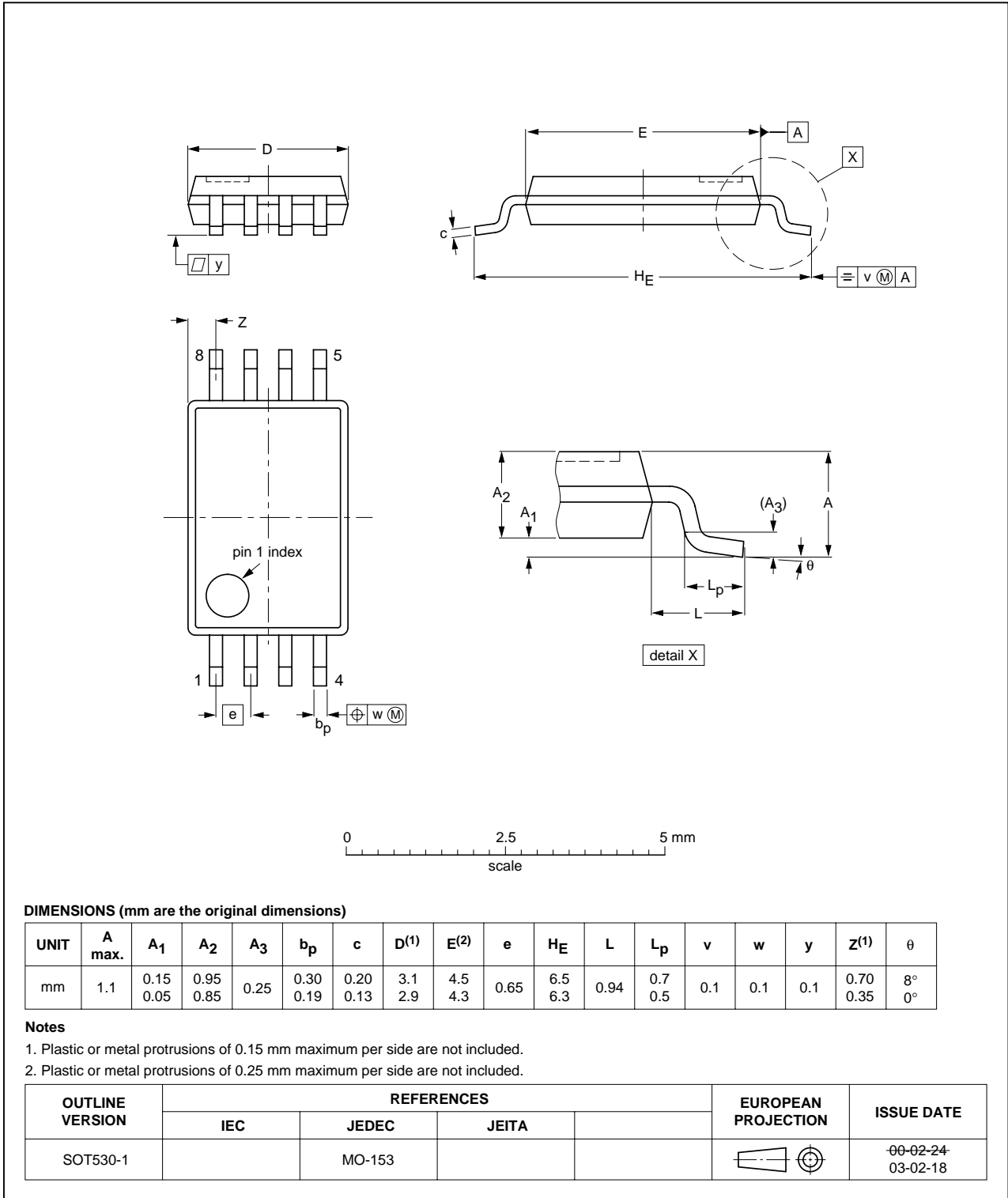


Fig 14. Package outline SOT530-1 (TSSOP8)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMWD20XN_2	20050426	Product data sheet	-	9397 750 14721	PMWD20XN-01
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • I_D and P_{tot} data revised in Section 1.4 “Quick reference data”. • I_D, I_{DM}, P_{tot}, I_S and I_{SM} data revised in Table 3 “Limiting values”. • Figure 3 revised in Section 4 “Limiting values”. • $R_{th(j-sp)}$ data revised in Table 4 “Thermal characteristics”. • Figure 4 revised in Section 5 “Thermal characteristics”. 				
PMWD20XN-01	20040119	Product data	-	9397 750 12595	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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