W83627EHF/EF

W83627EHG/EG

WINBOND LPC I/O

Date : November/16/2006 Revision :1.3

winbond

Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1		10/01/2004	0.5	N/A	First published preliminary version.
2		11/09/2004	0.51	N/A	Correct typo at 5.11.
3		12/07/2004	0.52	N/A	1. Correct DC CHARACTERISTICS description 2. Update Demo Circuit 3. Add Pb-free part no:W83627EHG
4		03/18/2005	0.6	N/A	Add SMART FAN™ III description
5		06/10/2005	0.61	N/A	Update application circuit
6		07/06/2005	0.62	N/A	Add new part W83627EF and W83627EG.
7		07/19/2005	0.63	N/A	Update pin configuration and application circuit
8		9/13/2005	1.0	N/A	Correct information and add AC Power Loss Timing chart
9	P.18	02/14/2006	1.1	N/A	Correct LPT function pins description.
10	P.79; P.80	08/04/2006	1.2	N/A	Remove “2N3904 activation” selection
11	P.103, P.104	11/16/2006	1.3	N/A	Correct description of CRF0 of Logical Device 2/3 (UARTA/B)

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Table of Contents-

1. GENERAL DESCRIPTION

W83627EHF/EHG/EF/EG is an evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (Low Pin Count) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83627EHF/EHG/EF/EG include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83627EHF/EHG/EF/EG greatly reduces the number of components required for interfacing with floppy disk drives. W83627EHF/EHG/EF/EG supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

W83627EHF/EHG/EF/EG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps which support higher speed modems. In addition, W83627EHF/EHG/EF/EG provides IR functions: IrDA 1.0 (SIR for 1.152K bps) .

W83627EHF/EHG/EF/EG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). And W83627EHF/EHG/EF/EG contains a Game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, they are very important for a entertainment or consumer computer.

W83627EHF/EHG/EF/EG provides Serial Flash ROM interface. That can support up to 8M bits serial flash ROM.

W83627EHF/EHG/EF/EG provides flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83627EHF/EHG supports hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly. Moreover, W83627EHF/EHG supports the Smart Fan control system, including the "Thermal Cruise™" and "Speed Cruise™" functions. Smart Fan can make system more stable and user friendly.

W83627EHF/EHG/EF/EG is made to fully comply with Microsoft© PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The special characteristic of Super I/O product line is to avoid power rails short. This is especially true to a multi-power system where power partition is much more complex than a single-power one. Special care might be applied during layout stage or the IC will fail even though its intended function is workable.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ#(LPC DMA), SERIRQ (Serial IRQ)
- Integrated Hardware Monitor functions
- Compliant with Microsoft PC2000/PC2001 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input
- It is 3.3V level but 5V tolerance support

  --- Besides LPC function pins(Pin21 ~ Pin30) and H/W monitor analog pins(Pin95 ~ Pin110)

  --- Input level can up to 5V and maximum input level can be up to 5V+10%

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Win95/98 driver

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:

  --- 5, 6, 7 or 8-bit characters

  --- Even, odd or no parity bit generation/detection

  --- 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities:

  --- Loop-back controls for communications link fault isolation

  --- Break, parity, overrun, framing error simulation

- Programmable baud rate generator allows division of 1.8461 MHz and 24 MHz by 1 to (216-1)
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axis (X, Y) and two button (A, B) controllers

MIDI Port

- The baud rate is 31.25 K baud
- 16-byte input FIFO
- 16-byte output FIFO

Keyboard Controller

- 8042 based with optional F/W from AMIKKEYTM-2, Phoenix MultiKey/42TM or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

Serial Flash ROM Interface

- Support up to 8M bits flash ROM

General Purpose I/O Ports

- 48 programmable general purpose I/O ports
- GPIO port 1 and 4 can not only serve as simple I/O ports but also watch dog timer output, Power LED output, Suspend LED output
- Functional in power down mode (GP24 ~ GP27, GPIO-3, GPIO-4, GPIO-5)

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

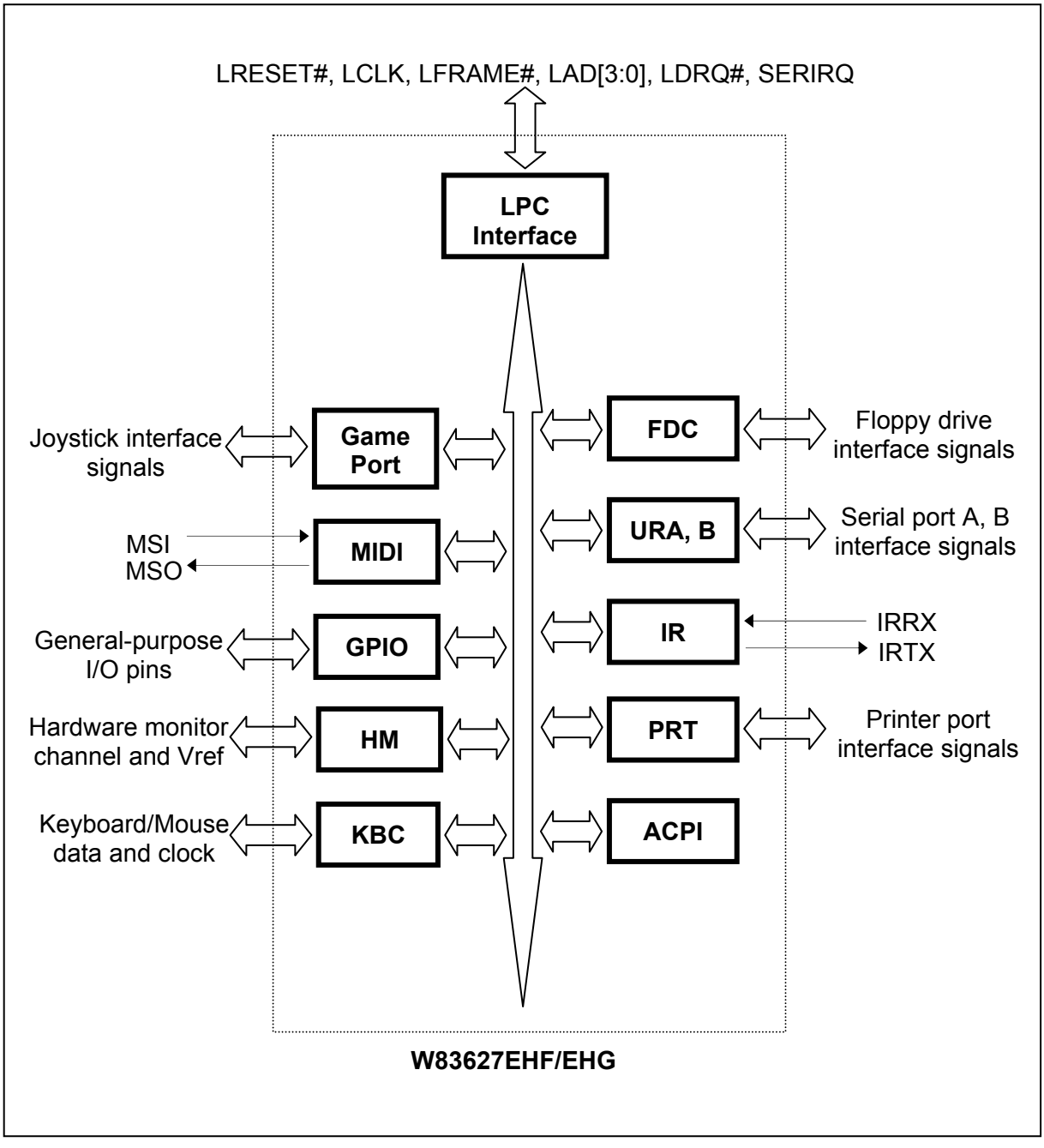
Hardware Monitor Functions (For W83627EHF/EHG only)

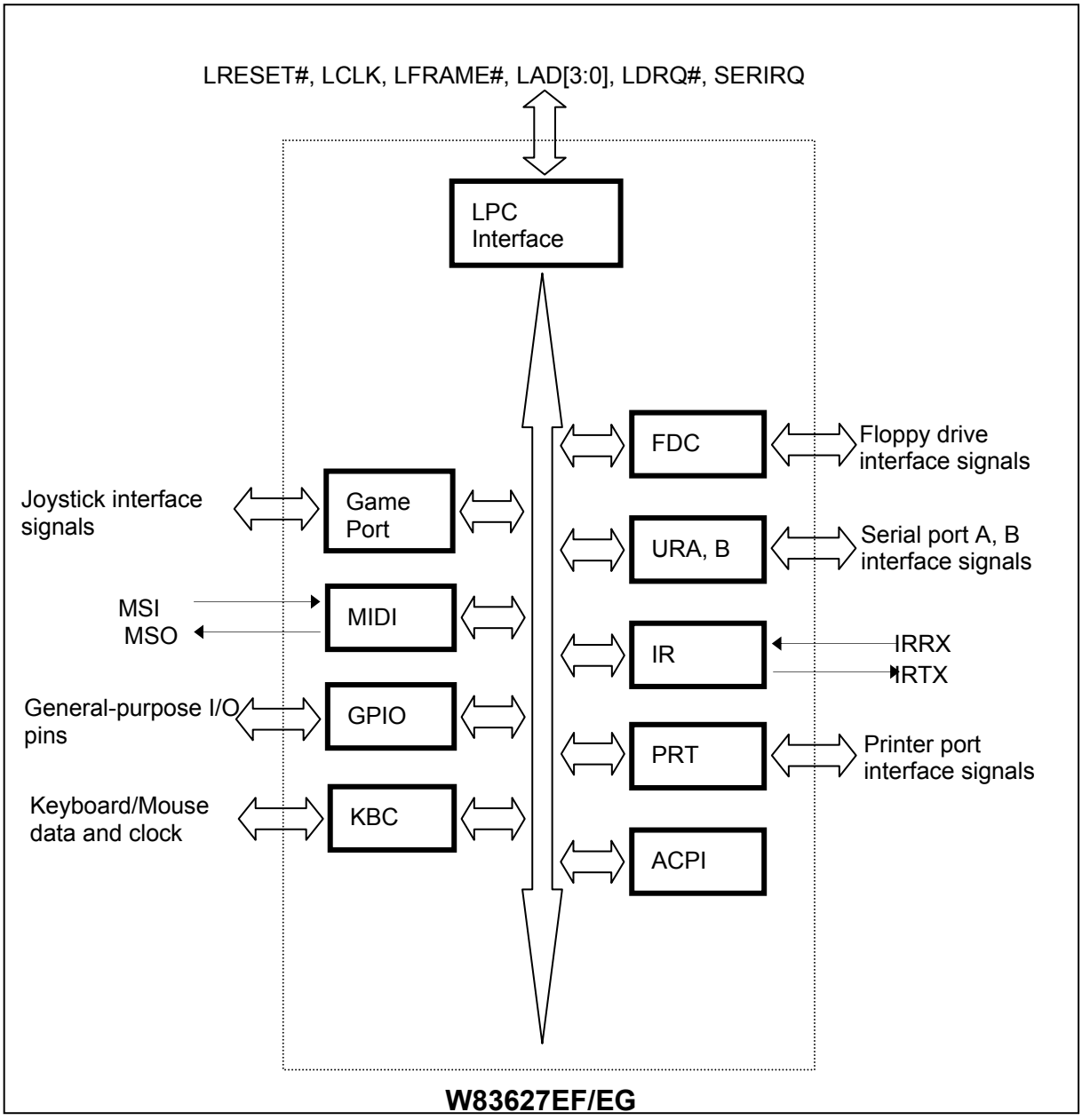
- Smart Fan control system, support SMART FANTM I - "Thermal CruiseTM" and "Speed CruiseTM" Mode , SMART FANTM III function
- 3 thermal inputs from optionally remote thermistors or entiumTM II/III/4 thermal diode output
- 10 voltage inputs (CPUVCORE, VIN[0..4] and intrinsic 3VCC, AVCC , 3VSB, VBAT)
- 5 fan speed monitoring inputs
- 4 fan speed control
- Dual mode for fan control (PWM & DC)
- Build in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over temperature indicate output
- Issue SMI#, OVT# to activate system protection
- Winbond Hardware DoctorTM Support
- 6 VID inputs / outputs
- Provide I2C interface to read/write registers

Package

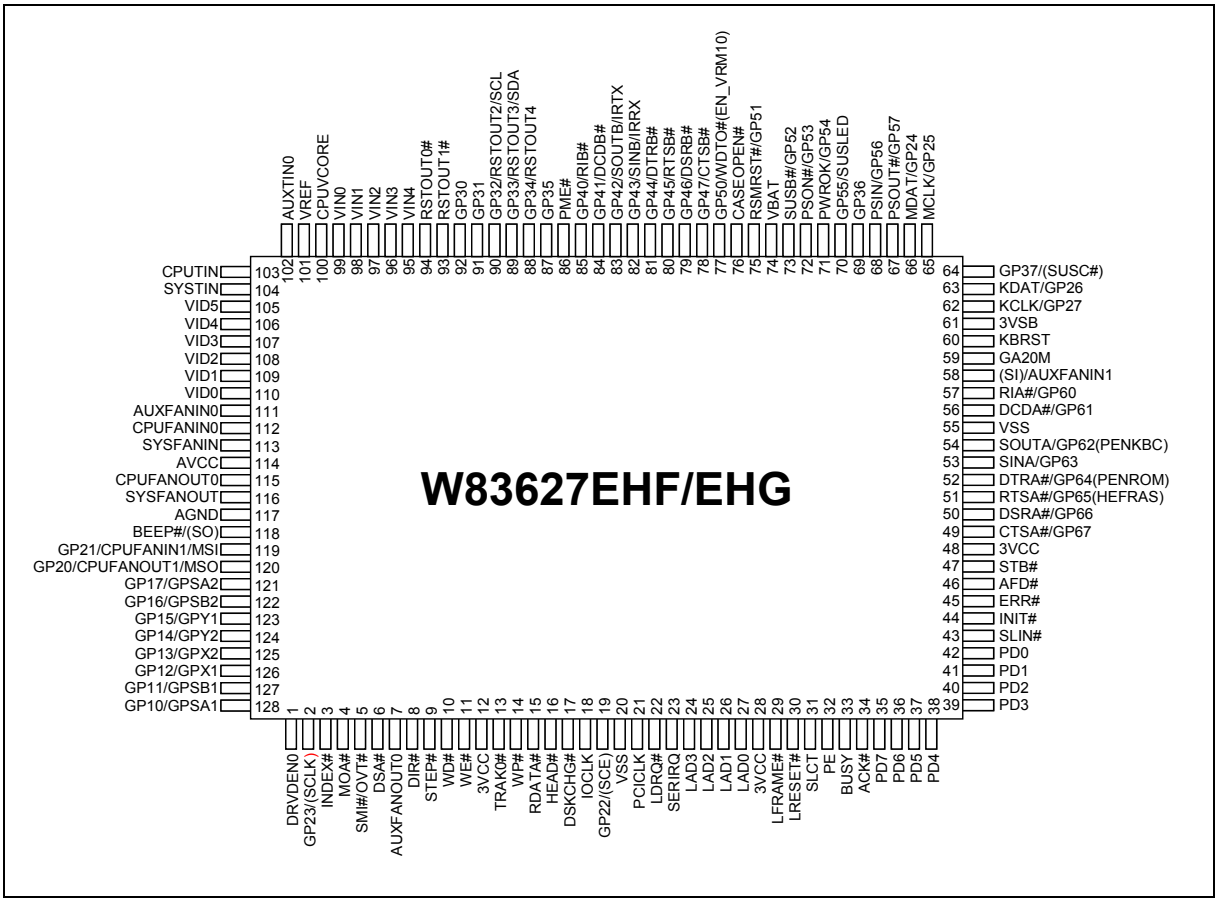
- 128-pin PQFP

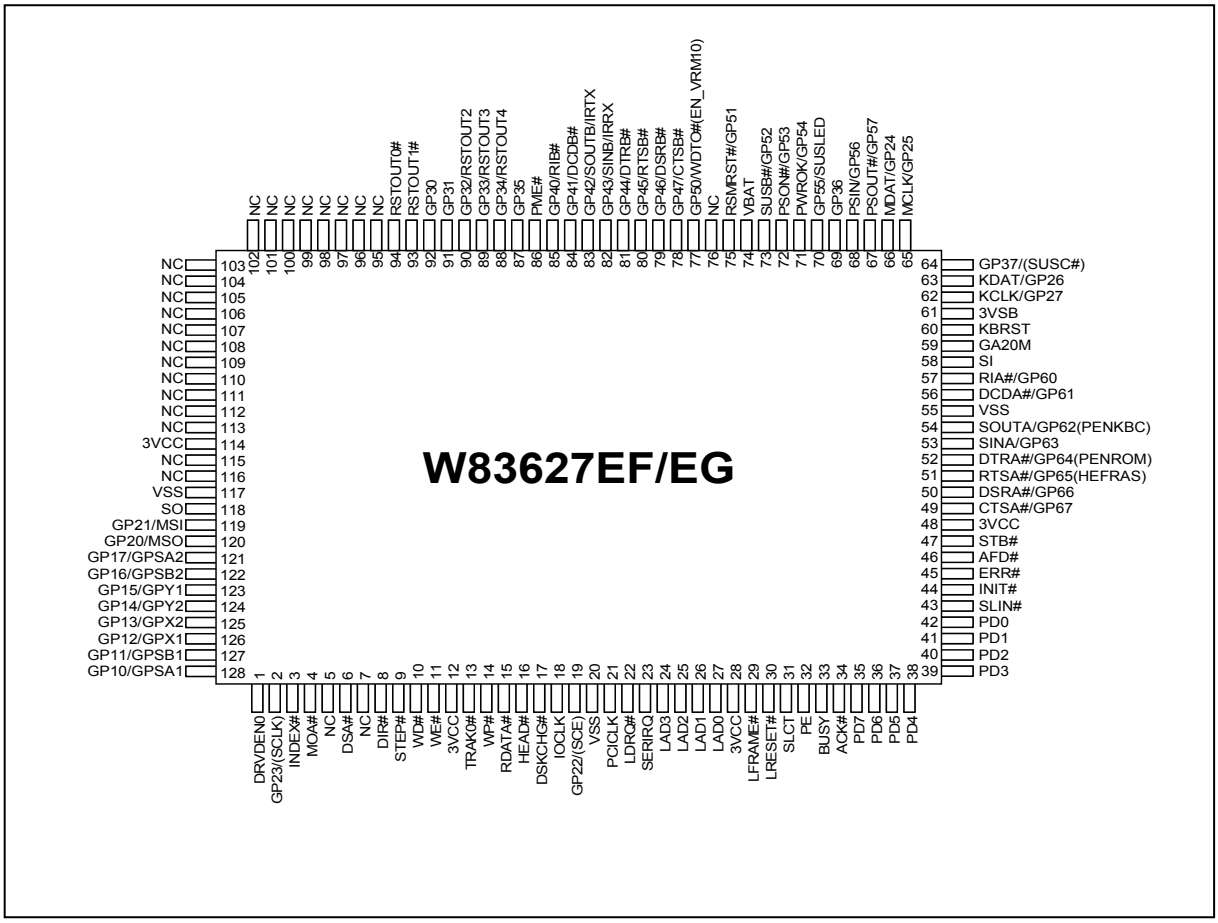
3. BLOCK DIAGRAM




LRESET#, LCLK, LFRAME#, LAD[3:0], LDRQ#, SERIRQ
LPC Interface
FDC
Floppy drive interface signals
Joystick interface signals
Game Port
URA, B
Serial port A, B interface signals
MSI
MSO
MIDI
IR
IRRX
IRTX
General-purpose I/O pins
GPIO
PRT
Printer port interface signals
Keyboard/Mouse data and clock
KBC
ACPI
W83627EF/EG

4. PIN CONFIGURATION




W83627EF/EG
1 DRVDEN0
2 GP23/(SCLK)
3 INDEX#
4 MOA#
5 NC
6 DSA#
7 NC
8 DIR#
9 STEP#
10 WD#
11 WE#
12 3VCC
13 TRAK0#
14 WP#
15 RDATA#
16 HEAD#
17 DSKCHG#
18 IOCLK
19 GP22/(SCE)
20 VSS
21 PCICLK
22 LDRQ#
23 SERIRQ
24 LAD3
25 LAD2
26 LAD1
27 LAD0
28 3VCC
29 LFRAME#
30 LRESET#
31 SLCT
32 PE
33 BUSY
34 ACK#
35 PD7
36 PD6
37 PD5
38 PD4
39 PD3
40 PD2
41 PD1
42 PD0
43 SLIN#
44 INIT#
45 ERR#
46 AFD#
47 STB#
48 3VCC
49 CTSA#/GP67
50 DSRA#/GP66
51 RTSA#/GP65(HEFRAS)
52 DTRA#/GP64(PENROM)
53 SINA/GP63
54 SOUTA/GP62(PENKBC)
55 VSS
56 DCDA#/GP61
57 RIA#/GP60
58 SI
59 GA20M
60 KBRST
61 3VSB
62 KCLK/GP27
63 KDAT/GP26
64 GP37/(SUSC#)
65 MCLK/GP25
66 MDAT/GP24
67 PSOUT#/GP57
68 PSIN/GP56
69 GP36
70 GP55/SUSLED
71 PWROK/GP54
72 PSON#/GP53
73 SUSB#/GP52
74 VBAT
75 RSMRST#/GP51
76 NC
77 GP50/WDTO#(EN_VRM10)
78 GP47/CTSB#
79 GP46/DSRB#
80 GP45/RTSB#
81 GP44/DTRB#
82 GP43/SINB/IRRX
83 GP42/SOUTB/IRTX
84 GP41/DCDB#
85 GP40/RIB#
86 PME#
87 GP35
88 GP34/RSTOUT4
89 GP33/RSTOUT3
90 GP32/RSTOUT2
91 GP31
92 GP30
93 RSTOUT1#
94 RSTOUT0#
95 NC
96 NC
97 NC
98 NC
99 NC
100 NC
101 NC
102 NC
103 NC
104 NC
105 NC
106 NC
107 NC
108 NC
109 NC
110 NC
111 NC
112 NC
113 NC
114 3VCC
115 NC
116 NC
117 VSS
118 SO
119 GP21/MSI
120 GP20/MSO
121 GP17/GPSA2
122 GP16/GPSB2
123 GP15/GPY1
124 GP14/GPY2
125 GP13/GPX2
126 GP12/GPX1
127 GP11/GPSB1
128 GP10/GPSA1

5. PIN DESCRIPTION

Note: Please refer to Section 8.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{cs} - CMOS level Schmitt-triggered input pin
IN_{t} - TTL level input pin
IN_{td} - TTL level input pin with internal pull down resistor
IN_{ts} - TTL level Schmitt-triggered input pin
IN_{tsp3} - 3.3V TTL level Schmitt-triggered input pin
IN_{tu} - TTL level input pin with internal pull up resistor
I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability
I/O_{12t} -3.3V TTL level bi-directional pin with 12 mA source-sink capability
I/OD_{12ts} - 3.3V TTL level bi-directional Schmitt-triggered pin. Open-drain output with 12 mA sink capability
I/OD_{16cs} - CMOS level Schmitt-triggered bi-directional pin. Open-drain output with 16 mA sink capability
I/OD_{24t} - TTL level bi-directional pin. Open-drain output with 24 mA sink capability
OUT_{8} - TTL level output pin with 8 mA source-sink capability
OUT_{12} -3.3V TTL level output pin with 12 mA source-sink capability
OUT_{24} - TTL level output pin with 24 mA source-sink capability
OD_{8} - Open-drain output pin with 8 mA sink capability
OD_{12} - Open-drain output pin with 12 mA sink capability
OD_{24} - Open-drain output pin with 24 mA sink capability

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
IOCLK	18	IN_{t}	System clock input, which is selective by the register according to the input frequency either 24MHz or 48MHz. Default is 48MHz.
PME#	86	OD_{12}	Generated PME event.
PCICLK	21	IN_{ts}	PCI clock 33 MHz input.
LDRQ#	22	O_{12}	Encoded DMA Request signal.
SERIRQ	23	I/OD_{12t}	Serial IRQ Input/Output.
LAD[3:0]	24-27	I/O_{12t}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	30	IN_{ts}	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	3	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
MOA#	4	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	13	IN_{csu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
WP#	14	IN_{csu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
RDATA#	15	IN_{csu}	The read data input signal from the FDD. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
HEAD#	16	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	17	IN_{csu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin can be pulled up internally by a 1 KΩ(±50%) . The resistor also can be disabled/enabled by bit 7 of LD0-CRF0 (FIPURDWN). Default is disabled.

5.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	FUNCTION
SLCT	31	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
PE	32	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
BUSY	33	IN_{ts}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
SLIN#	43	OD_{12} $/OUT_{12}$	PRINTER MODE: SLIN# Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INIT#	44	OD_{12} $/OUT_{12}$	PRINTER MODE: INIT# Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
AFD#	46	OD_{12} $/OUT_{12}$	PRINTER MODE: AFD# An activtput from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STB#	47	OD_{12} $/OUT_{12}$	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

Multi-Mode Parallel Port, continued.

SYMBOL	PIN	I/O	FUNCTION
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

5.4 Serial Port & Infrared Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA#	49	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP67		I/OD_{12t}	General purpose I/O port 6 bit 7.
CTSB#	78	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47***		I/OD_{12t}	General purpose I/O port 4 bit 7.
DSRA#	50	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP66		I/OD_{12t}	General purpose I/O port 6 bit 6.

Serial Port & Infrared Port Interface, Continued.

SYMBOL	PIN	I/O	FUNCTION
DSRB#	79	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46*		I/OD_{12t}	General purpose I/O port 4 bit 6.
RTSA#	51	OUT_8	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN_t	During power-on reset, this pin is pulled down internally(20K± 30%) and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
GP65		I/O_8	General purpose I/O port 6 bit 5.
RTSB#	80	OUT_8	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
GP45***		I/OD_{8t}	General purpose I/O port 4 bit 5.
DTRA#	52	OUT_8	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.
PENROM		IN_t	During power-on reset, this pin is pulled down internally(20K ± 30%)and is defined as PENROM disable, which provides the power-on value for CR24 bit 1 (ENROM). A 1 kΩ is reserved to pull down and a 1 kΩ resistor is recommended if intends to pull-up to enable ROM.
GP64		I/O_8	General purpose I/O port 6 bit 4.
DTRB#	81	OUT_8	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
GP44*		I/OD_{8t}	General purpose I/O port 4 bit 4.
SINA	53	IN_t	Serial Input. It is used to receive serial data through the communication link.
GP63		I/OD_8	General purpose I/O port 6 bit 3.
SINB	82	IN_t	Serial Input. It is used to receive serial data through the communication link.
IRRX			IR Receiver input.
GP43***		I/OD_{12}	General purpose I/O port 4 bit 3.

Serial Port & Infrared Port Interface, Continued.

SYMBOL	PIN	I/O	FUNCTION
SOUTA	54	OUT_8	UART A Serial Output. It is used to transmit serial data out to the communication link.
PENKBC		IN_t	During power on reset, this pin is pulled down internally(20K ± 30%)and is defined as PENKBC, which provides the power on value for CR24 bit 2. A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up.
GP62		I/O_8	General purpose I/O port 6 bit 2.
SOUTB	83	OUT_8	UART B Serial Output. It is used to transmit serial data out to the communication link.
IRTX			IR Transmitter output.
GP42*		I/OD_8	General purpose I/O port 4 bit 2.
DCDA#	56	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP61		I/OD_{12}	General purpose I/O port 6 bit 1.
DCDB#	84	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP41***		I/OD_{12}	General purpose I/O port 4 bit 1.
RIA#	57	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP60	57	I/OD_{12}	General purpose I/O port 6 bit 0.
RIB#	85	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP40*		I/OD_12	General purpose I/O port 4 bit 0.

Note. The * sign see 5.10.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

5.5 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
GA20M	59	OUT_{12}	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST	60	OUT_{12}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	62	I/OD_{16ts}	Keyboard Clock.
GP27		I/OD_{16t}	General purpose I/O port 2 bit 7.
KDAT	63	I/OD_{16ts}	Keyboard Data.
GP26		I/OD_{16t}	General purpose I/O port 2 bit 6.
MCLK	65	I/OD_{16ts}	PS2 Mouse Clock.
GP25		I/OD_{16t}	General purpose I/O port 2 bit 5.
MDAT	66	I/OD_{16ts}	PS2 Mouse Data.
GP24		I/OD_{16t}	General purpose I/O port 2 bit 4.

5.6 Serial Flash Interface

SYMBOL	PIN	I/O	FUNCTION
SCE#	19	OUT_{12}	Serial Flash ROM interface chip select.
GP22		I/OD_{12t}	General purpose I/O port 2 bit 2.
SCK	2	OUT_{12}	Clock output for Serial Flash. (33MHz)
GP23		I/OD_{12t}	General purpose I/O port 2 bit 3.
SO	118	OUT_{8}	Transfer commands, address or data to Serial Flash. It is connected to SI of Serial Flash.
BEEP		OD_{8}	Beep function for hardware monitor. This pin is low after system reset.**(for H version only, C version is tri- state)**
SI	58	IN_{ts}	Receive data from Serial Flash. It is connected to SO of Serial Flash.
AUXFANIN1		I/O_{12ts}	0 to +3V amplitude fan tachometer input.

5.7 Hardware Monitor Interface

SYMBOL	PIN	I/O	FUNCTION
BEEP	118	OD_8	Beep function for hardware monitor. This pin is low after system reset. **(for H version only, C version is tri-state)**
SO		OUT_8	Transfer commands, address or data to Serial Flash. It is connected to SI of Serial Flash.
CASEOPEN#	76	IN_t	CASE OPEN detected. An active low level input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83627EHF/EHG is power off. This pin is VSS for W83627EF/EG.**Pull down is recommended if useless**. **(For H version only, C version is falling edge trigger only)**
VIN4	95	AIN	0V to 2.048V FSR Analog Inputs. (FSR: Full Scale Register)
VIN3	96	AIN	0V to 2.048V FSR Analog Inputs.
VIN2	97	AIN	0V to 2.048V FSR Analog Inputs.
VIN1	98	AIN	0V to 2.048V FSR Analog Inputs.
VIN0	99	AIN	0V to 2.048V FSR Analog Inputs.
CPUVCORE	100	AIN	0V to 2.048V FSR Analog Inputs.
VREF	101	AOUT	Reference Voltage (2.048V) for temperature maturation.
AUXTIN	102	AIN	Temperature sensor 3 inputs. It is used for temperature maturation.
CPUTIN	103	AIN	Temperature sensor 2 inputs. It is used for CPU temperature maturation.
SYSTIN	104	AIN	Temperature sensor 1 input. It is used for system temperature maturation.
OVT#	5	OD_{12}	Over temperature Shutdown Output. It indicated the temperature is over temperature limit.
HM_SMI#		OD_{12}	System Management Interrupt channel output. (Default after PCIRST)
VID5 VID4 VID3 VID2 VID1 VID0	105 106 107 108 109 110	I/O_{12}	VID input detect, also with output control.
AUXFANIN1	58	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
SI		IN_{ts}	Receive data from Serial Flash. It is connected to SO of Serial Flash.

Hardware Monitor Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
AUXFANIN0 CPUFANIN0 SYSFANIN	111 112 113	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
CPUFANIN1	119	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input. (Default)
MSI		IN_{cs}	MIDI serial data input.
GP21		I/OD_{12t}	General purpose I/O port 2 bit 1.
AUXFANOUT CPUFANOUT0 SYSFANOUT	7 115 116	AOUT/ OD_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode. (For H version, while SYSFANOUT or CPUFANOUT0 be selected to PWM Mode, either of them can be open-drain or push-pull output. The controlled bits are CR24h bit[4:3]. Open-drain output is default.)
CPUFANOUT1	120	AOUT/ OUT_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
MSO		OUT_{12}	MIDI serial data output.
GP20		I/OD_{12t}	General purpose I/O port 2 bit 0.

5.8 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
GPSA1	128	IN_{cs}	Active-low, Joystick I switch input 1. (Default)
GP10*		I/OD_{12cs}	General purpose I/O port 1 bit 0.
GPSB1	127	IN_{cs}	Active-low, Joystick II switch input 1. (Default)
GP11**		I/OD_{12cs}	General purpose I/O port 1 bit 1.
GPX1	126	I/OD_{12cs}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP12*			General purpose I/O port 1 bit 2.
GPX2	125	I/OD_{12cs}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP13**			General purpose I/O port 1 bit 3.

Game Port & MIDI Port, continued.

SYMBOL	PIN	I/O	FUNCTION
GPY2	124	I/OD_{12cs}	Joystick II timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP14*			General purpose I/O port 1 bit 4.
GPY1	123	I/OD_{12cs}	Joystick I timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP15**			General purpose I/O port 1 bit 5.
GPSB2	122	IN_{cs}	Active-low, Joystick II switch input 2. (Default)
GP16*		I/OD_{12cs}	General purpose I/O port 1 bit 6.
GPSA2	121	IN_{cs}	Active-low, Joystick I switch input 2. (Default)
GP17**		I/OD_{12cs}	General purpose I/O port 1 bit 7.
MSI	119	IN_{cs}	MIDI serial data input. (Default)
CPUFANIN1		I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
GP21		I/OD_{12t}	General purpose I/O port 2 bit 1.
MSO	120	OUT_{12}	MIDI serial data output. (Default)
CPUFANOUT1		AOUT/ OUT_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
GP20		I/OD_{12t}	General purpose I/O port 2 bit 0.

Note. The * sign see 5.10.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

5.9 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
PSIN	68	IN_{td}	Panel Switch Input. This pin is high active with an internal pull down resistor.
GP56		I/OD_{12t}	General purpose I/O port 5 bit 6.
PSOUT#	67	OD_{12}	Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low.
GP57		I/OD_{12t}	General purpose I/O port 5 bit 7.
VBAT	74	PWR	+3.3V on-board battery for the digital circuitry.
RSTOUT0#	94	OD_{12}	Secondary LRESET# output 0.
RSTOUT1#	93	OUT_{12}	Secondary LRESET# output 1.
RSTOUT2#	90	OUT_{12}	Secondary LRESET# output 2.
GP32		I/OD_{12t}	General purpose I/O port 3 bit 2.
SCL		IN_{ts}	Serial Bus clock.
RSTOUT3#	89	OUT_{12}	Secondary LRESET# output 3.
GP33		I/OD_{12t}	General purpose I/O port 3 bit 3.
SDA		I/OD_{12ts}	Serial bus bi-directional Data.
RSTOUT4#	88	OUT_{12}	Secondary LRESET# output 4.
GP34		I/OD_{12t}	General purpose I/O port 3 bit 4.

5.10 General Purpose I/O Port

5.10.1 GPIO Power Source

SYMBOL	POWER SOURCE
GPIO port 1	VCC
GPIO port 2 (Bit0-3)	VCC
GPIO port 2 (Bit4-7)	VSB
GPIO port 3	VSB
GPIO port 4	VSB
GPIO port 5	VSB
GPIO port 6	VCC

5.10.2 GPIO-1 Interface

see 5.8 Game Port

5.10.3 GPIO-2 Interface

SYMBOL	PIN	I/O	FUNCTION
GP20	120	I/OD_{12t}	General purpose I/O port 2 bit 0.
CPUFANOUT1		AOUT/ OUT_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
MSO		OUT_{12}	MIDI serial data output. (Default)
GP21	119	I/OD_{12t}	General purpose I/O port 2 bit 1.
CPUFANIN1		I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
MSI		IN_{cs}	MIDI serial data input. (Default)
GP22	19	I/OD_{12t}	General purpose I/O port 2 bit 2.
SCE#		OUT_{12}	Serial Flash ROM interface chip select.
GP23	2	I/OD_{12t}	General purpose I/O port 2 bit 3.
SCK		OUT_{12}	Clock output for Serial Flash. (33MHz)
GP24	66	I/OD_{16t}	General purpose I/O port 2 bit 4.
MDAT		I/OD_{16ts}	PS2 Mouse Data.
GP25	65	I/OD_{16t}	General purpose I/O port 2 bit 5.
MCLK		I/OD_{16ts}	PS2 Mouse Clock.
GP26	63	I/OD_{16t}	General purpose I/O port 2 bit 6.
KDAT		I/OD_{16ts}	Keyboard Data.
GP27	62	I/OD_{16t}	General purpose I/O port 2 bit 7.
KCLK		I/OD_{16ts}	Keyboard Clock.

5.10.4 GPIO-3 Interface

SYMBOL	PIN	I/O	FUNCTION
GP30	92	I/OD_{12t}	General purpose I/O port 3 bit 0.
GP31	91	I/OD_{12t}	General purpose I/O port 3 bit 1
GP32	90	I/OD_{12t}	General purpose I/O port 3 bit 2.
RSTOUT2#		OUT_{12}	Secondary LRESET# output 2.
SCL		IN_{ts}	Serial Bus clock.
GP33	89	I/OD_{12t}	General purpose I/O port 3 bit 3.
RSTOUT3#		OUT_{12}	Secondary LRESET# output 3.
SDA		I/OD_{12ts}	Serial bus bi-directional Data.
GP34	88	I/OD_{12t}	General purpose I/O port 3 bit 4.
RSTOUT4#		OUT_{12}	Secondary LRESET# output 4.
GP35	87	I/OD_{12t}	General purpose I/O port 3 bit 5
GP36	69	I/OD_{12t}	General purpose I/O port 3 bit 6
GP37	64	I/OD_{12t}	General purpose I/O port 3 bit 7

5.10.5 GPIO-4 Interface

see 5.4 Serial Port B

5.10.6 GPIO-5 Interface

SYMBOL	PIN	I/O	FUNCTION
GP50	77	I/O_{12t}	General purpose I/O port 5 bit 0.
EN_VRM10		IN_{cd}	During VSB power reset (RSMRST), this pin is pulled down internally and is defined as VID transition voltage level, which provides the value for CR2C bit 3. A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up.
WDTO#		OUT_{12}	Watchdog timer output signal.
GP51	75	I/OD_{12t}	General purpose I/O port 5 bit 1.
RSMRST#		OD_{12}	Resume reset signal output.
GP52	73	I/OD_{12t}	General purpose I/O port 5 bit 2.
SUSB#		IN_t	System S3 states input.
GP53	72	I/OD_{12t}	General purpose I/O port 5 bit 3.
PSON#		OD_{12}	This pin generates the PWRCTL# signal while the power failure.
GP54	71	I/OD_{12t}	General purpose I/O port 5 bit 4.
PWROK		OD_{12}	This pin generates the PWROK signal while the VCC come in.

GPIO-5 Interface, continued.

SYMBOL	PIN	I/O	FUNCTION
GP55	70	I/O_{12t}	General purpose I/O port 5 bit 5. (This pin is push-pull output mode)
SUSLED		OUT_{12}	Suspended LED output. (This pin is push-pull output mode)
GP56	68	I/OD_{12t}	General purpose I/O port 5 bit 6.
PSIN		IN_{td}	Panel Switch Input. This pin is high active with an internal pull down resistor.
GP57	67	I/OD_{12t}	General purpose I/O port 5 bit 7.
PSOUT#		OD_{12}	Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low.

5.10.7 GPIO-6 Interface

see 5.4 Serial Port A

5.10.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

SYMBOL	PIN	I/O	FUNCTION
GPxx*	---	I/OD_{12t}	This GPxx* can be served GPIO or Watchdog timer output signal.
WDTO#		OD_{12}	
GPxx**	---	I/OD_{12t}	This GPxx** can be served GPIO or Power LED output signal.
PLED		OD_{12}	
GPxx***	---	I/OD_{12t}	This GPxx*** can be served GPIO or Suspend LED output signal.
SUSLED		OD_{12}	

5.11 POWER PINS

SYMBOL	PIN	FUNCTION
3VSB	61	+3.3V stand-by power supply for the digital circuitry.
VBAT	74	+3V on-board battery for the digital circuitry.
3VCC	12,28,48	+3.3V power supply for driving 3V on host interface.
AVCC	114	Analog +3.3V power input. Internally supplier to all analog circuitry.
AGND	117	Internally connected to all analog circuitry. The ground reference for all analog inputs.
GND	20,55	Ground.

6. Hardware monitor

6.1 General Description

The W83627EHF/EHG can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stable and properly. W83627EHF/EHG provides LPC interface to access hardware.

An 8-bit analog-to-digital converter (ADC) was built inside W83627EHF/EHG. The W83627EHF/EHG can simultaneously monitor 6 analog voltage inputs (intrinsic monitor VBAT,3VSB, 3VCC,& AVCC power), 5 fan tachometer inputs, 3 remote temperature, one case-open detection signal. The remote temperature sensing can be performed by thermistors or directly from Intel™ Deschutes CPU thermal diode output. Also the W83627EHF/EHG provides: 4 PWM (pulse width modulation) outputs for the fan speed control or 4 DCFAN outputs for the fan speed control; beep tone output for warning; HM_SMI#(through SERIRQ or OVT# pin) , OVT# signals for system protection events.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Winbond's Hardware Doctor™ or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and masked interrupts. An optional beep tone could be used as warning signals when the monitored parameters are out of the preset range.

6.2 Access Interface

W83627EHF/EHG provides two interface for microprocessor to read/write hardware monitor internal registers.

6.2.1 LPC interface

The first interface uses LPC Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The other higher bits of these ports is set by W83627EHF/EHG itself. The general decoded address is set to port 295h and port 296h. These two ports are described as following:

Port 295h: Index port.

Port 296h: Data port.

The register structure is showed as the Figure 6.1

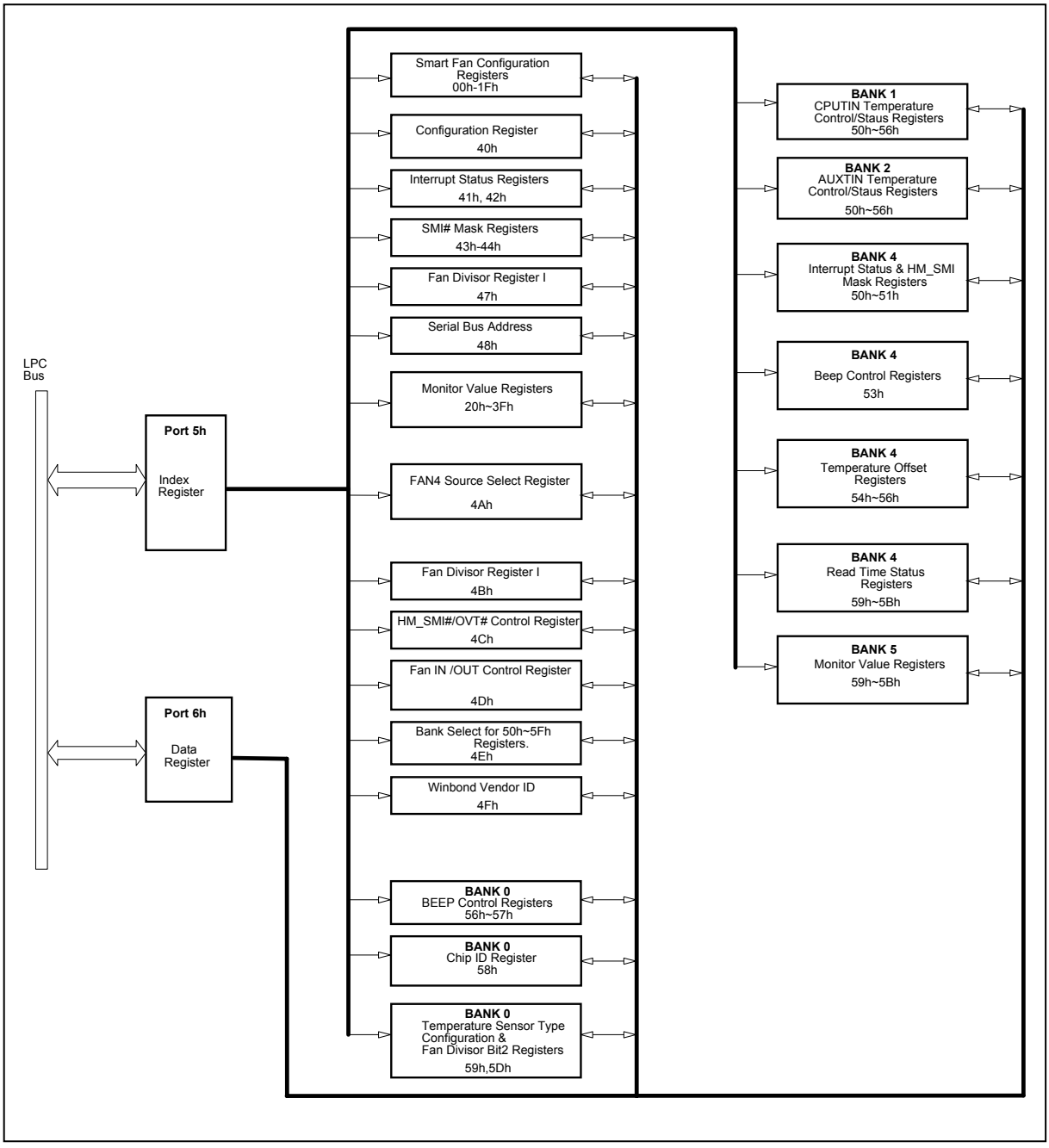


Figure 6.1 : LPC interface access diagram

6.2.2 I²C interface

The second interface uses I²C Serial Bus. W83627EHF/EHG has a programmable serial bus address. It defined at Index 48h.

6.2.2.1. Serial bus (I²C) access timing

(a) Serial bus write to internal address register followed by the data byte

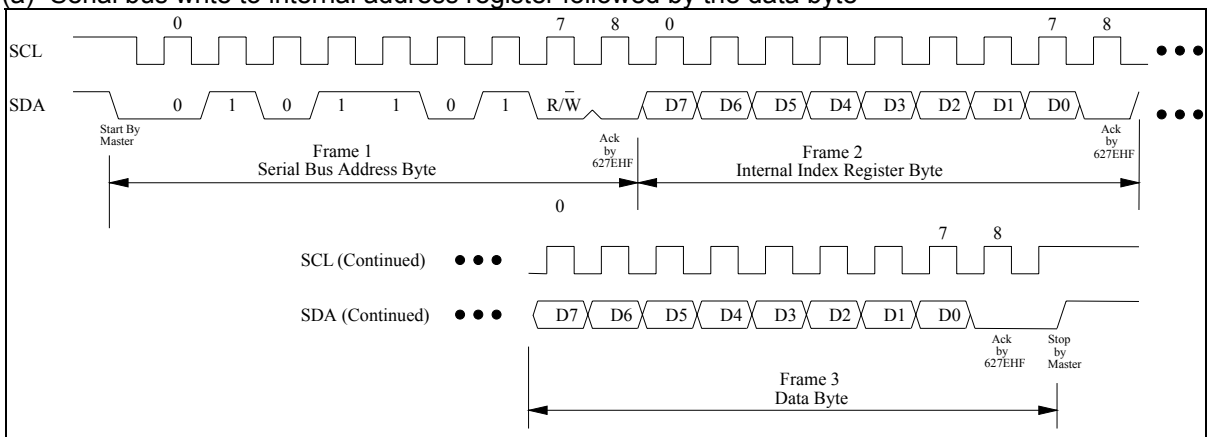


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read from a register

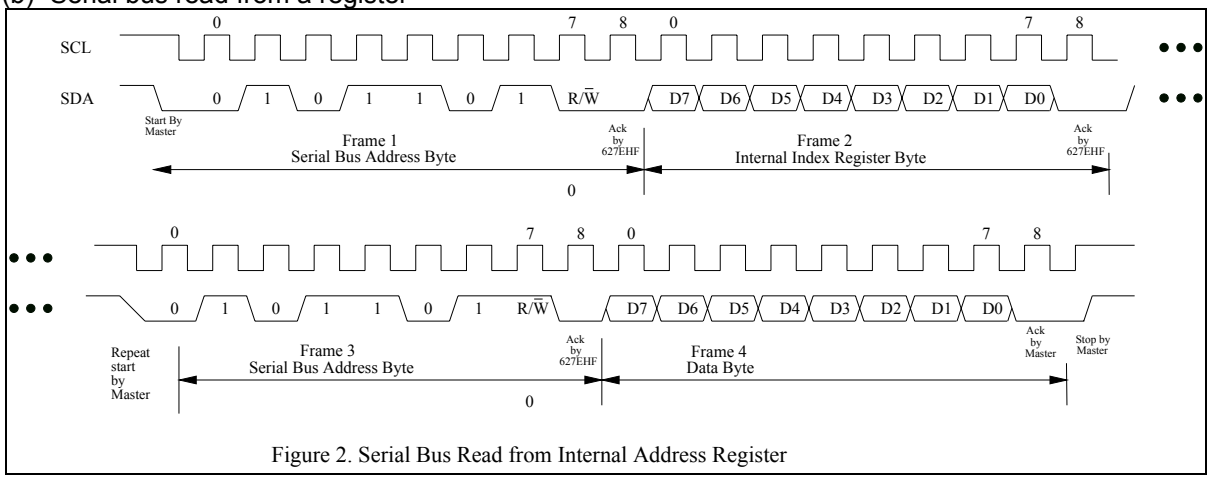


Figure 2. Serial Bus Read from Internal Address Register

6.3 Analog Inputs

The maximum input voltage of the analog pin is 2.048V because the 8-bit ADC has a 8mV LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU Vcore voltage , battery(pin 74), 3VSB(pin 61), 3VCC(pin 12) , AVCC(pin 114) voltage can directly connected to these analog inputs. The +12V voltage inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 6.2 shows.

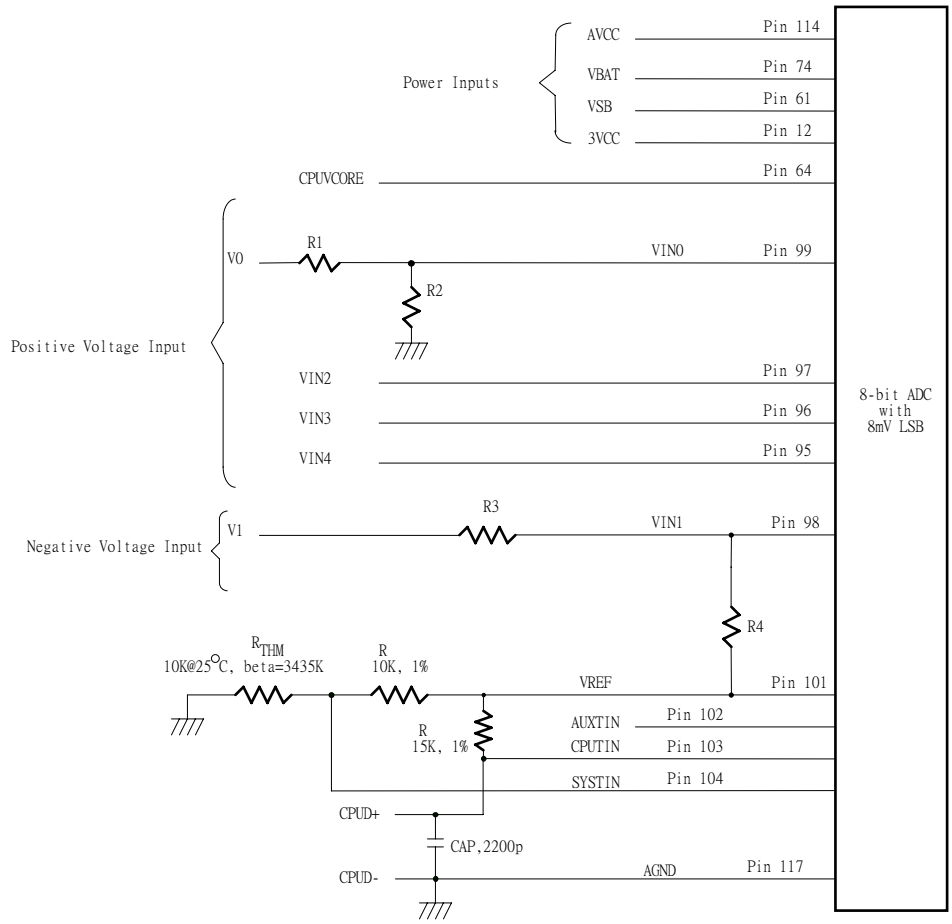


Figure 6.2

6.3.1 Monitor over 2.048V voltage

The +12V input voltage can be expressed as following equation.

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 56K Ohms and 10K Ohms, respectively, when the input voltage V_0 is 12V. The node voltage of VIN0 can be subject to less than 2.048V for the maximum input range of the 8-bit ADC.

The -12V input voltage can be expressed as following equation.

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

The value of R3 and R4 can be selected to 232K Ohms and 10K Ohms, respectively, when the input voltage V_1 is -12V. The node voltage of VIN1 can be subject to less than 2.048V for the maximum input range of the 8-bit ADC.

Both of pin 12 and pin 114 are connected to the power supply VCC with +3.3V. There are two functions in these 2 pins with 3.3V. The first function is to supply internal (digital/analog) power in the

W83627EHF/EHG and the second function is that this voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The W83627EHF/EHG internal two serial resistors are 34 KΩ and 34 KΩ so that input voltage to ADC is 1.65V which is less than 2.048V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V.

The Pin 61 is connected to 3.3 VSB voltage. W83627EHF/EHG monitors this voltage and the internal two serial resistors are 34 KΩ and 34 KΩ so that input voltage to ADC is 1.65V which less than 2.048V of ADC maximum input voltage.

6.3.2 CPUVCORE voltage detection method

W83627EHF/EHG provides one detection methods for CPUVCORE(pin 100).

The LSB of this mode is 8mV. This means that the detected voltage equals to the reading of this voltage register multiplies 8mV. The formula is as the following:

Detected Voltage = $\text{Reading} * 0.008$ V

6.3.3 Temperature Measurement Machine

The temperature data format is 8-bit two's-complement for sensor SYSTIN and 9-bit two's-complement for sensor CPUTIN and AUXTIN. The 8-bit temperature data can be obtained by reading the CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1/Bank2 CR[50h] and the LSB from the Bank1/Bank2 CR[51h] bit 7. The format of the temperature data is show in Table 6.1.

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Table 6.1

6.3.3.1. Monitor temperature from thermistor

The W83627EHF/EHG can connect three thermistors to measure three different environment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 6.2, the themistor is connected by a serial resistor with 10K Ohms, then connect to VREF (pin 101).

6.3.3.2. Monitor temperature from Pentium IITM/Pentium IIITM thermal diode

The W83627EHF/EHG can alternate the thermistor to Pentium II™/Pentium III™ thermal diode and the circuit connection is shown as Figure 6.3. The pin of Pentium II™/ Pentium III™ D- is connected to AGND(pin 117) and the pin D+ is connected to temperature sensor pin in the W83627EHF/EHG. The resistor R=15K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=2200pF should be added to filter the high frequency noise.

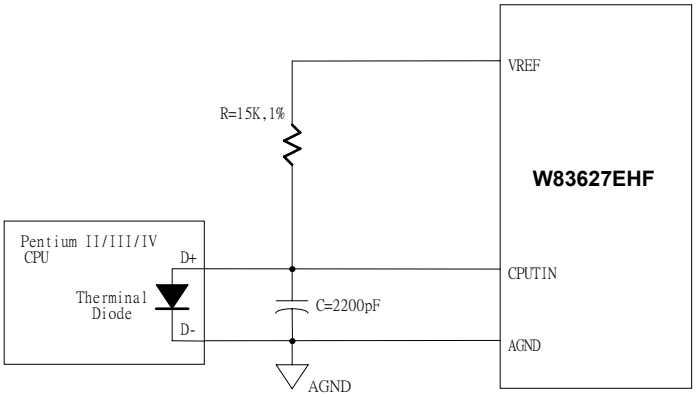


Figure 6.3

6.4 FAN Speed Count and FAN Speed Control

6.4.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over **+3.3V**. If the input signals from the tachometer outputs are over the **+3.3V**, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 6.4.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register Bank0 Index 28h, 29h, 2Ah ,3Fh and Bank5 53h, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at Bank0 Index 47h.bit7~4, Index 4Bh.bit7~6, Index 4Ch.bit7, Index 59h.bit7.bit3~2 and Index 5Dh.bit5~7 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, RPM, and count.

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.84 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

Table 6.2

6.4.2 Fan speed control

W83627EHF/EHG provides two controllable methods for Fan speed control. One is PWM duty cycle output and the other is DC voltage output. Either PWM or DC output can be programmed at Bank0 Index 04h.bit1~0 , Index 12h.bit0 and Index 62h.bit6.

6.4.2.1. PWM Duty Cycle Output

The W83627EHF/EHG provides maximum 4 sets for fan PWM speed control. The duty cycle of PWM can be programmed by a 8-bit registers which are defined in the Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The default duty cycle is set to **100%**, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Dutycycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The PWM clock frequency also can be program and defined in the Bank0 Index 00h, Index 02h, Index 10h and Index 60h.

6.4.2.2. DC Voltage Output

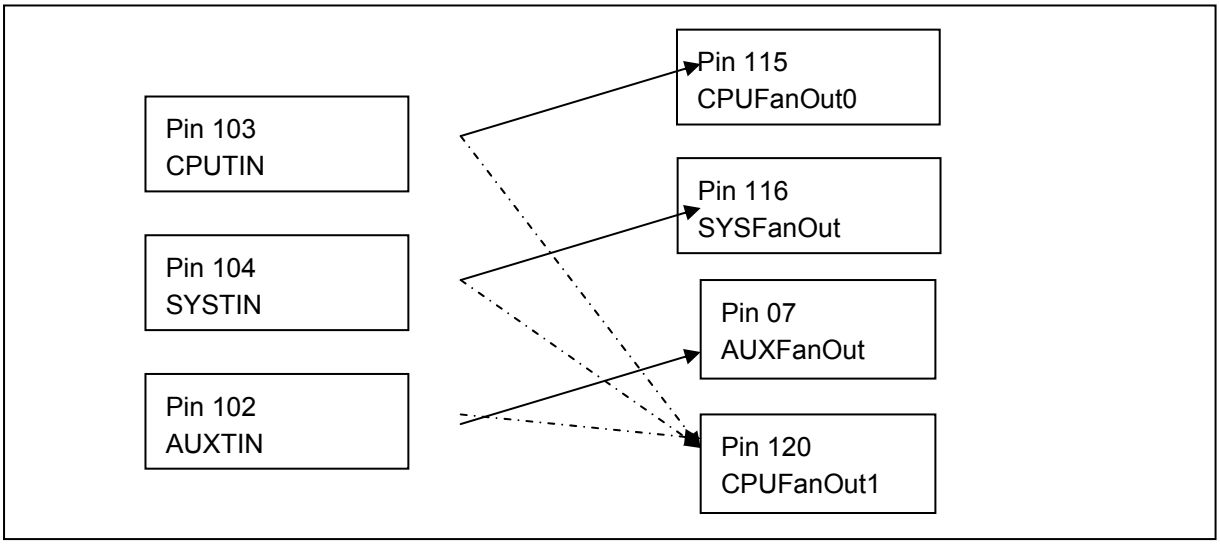
The W83627EHF/EHG has a 6 bit DAC which produces 0 to 3.3 volts DC output that provides maximum 4 sets for fan speed control. The analog output can be programmed in the Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The default value is 111111YY,YY is reserved 2 bits, that is default output value is nearly 3.3 V. The expression of output voltage can be represented as follow ,

$$\text{Output Voltage (V)} \quad = 3VCC \times \frac{\text{Programmed 6 - bit Register Value}}{64}$$

6.5 Smart Fan Control

SMART FAN™ I :

Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode. When enable Smart Fan, the Fan output will start from previous setting of Bank0 Index 01h, Index 03h, Index 11h and Index 61h to increase or decrease.



6.5.1 Thermal Cruise mode

There are maximum 4 pairs of Temperature/Fan output control at this mode: SYSTIN with SYSFANOUT, CPUTIN with CPUFANOUT0, AUXTIN with AUXFANOUT and CPUFANOUT1 depends on Bank0 Index 4Ah.bit7~6 setting that is temperature source selection.

W83627EHF/EHG provides the Smart Fan system which can control the fan speed automatically depend on current temperature to keep it with in a specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS, as long as the real temperature remains below the setting value, the fan will be off. Once the temperature exceeds the setting high limit temperature (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 20% output) and automatically controlled its output with the temperature varying. Three conditions may occur :

(1) If the temperature still exceeds the high limit (ex: 58°C), Fan output will increase slowly. If the fan has been operating in its fully speed but the temperature still exceeds the high limit(ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target area(ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), Fan output will decrease slowly to 0 until the temperature exceeds the low limit.

In other words, If “current temperature” > “High Limit”, increase fan speed;
If “current temperature” < “Low Limit”, decrease fan speed;
Otherwise, keep the fan speed.

Figure 6.6 PWM fan mode and Figure 6.7 DC fan mode illustrate the Thermal Cruise mode

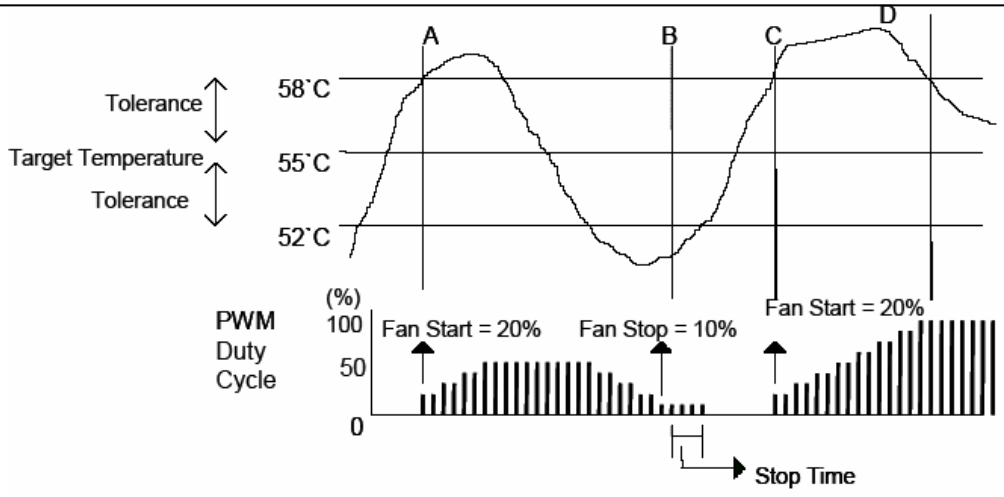


Figure 6.6

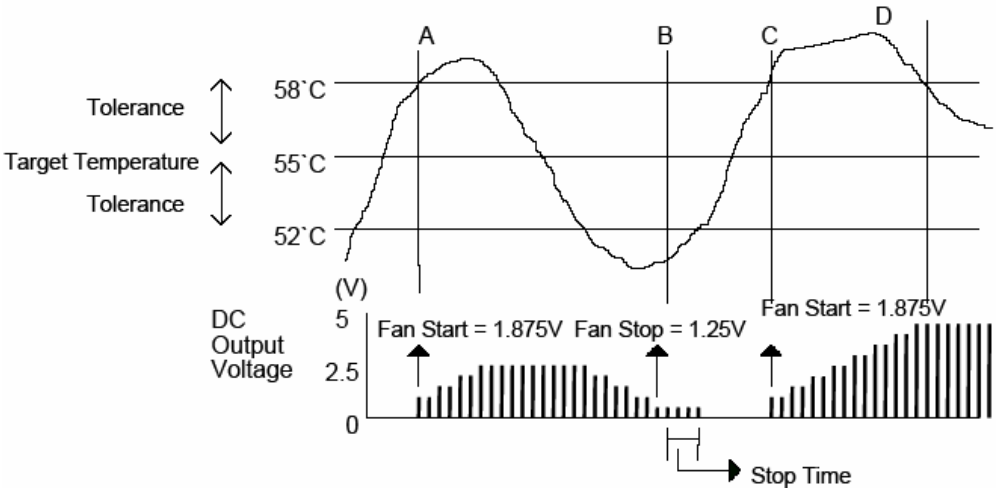


Figure 6.7

One more protection is provided that Fan output will not be decreased to 0 in the above (3) situation in order to keep the fans running with a minimum speed. By setting Bank0 Index12h.bit3~5 to 1, Fan output will be decreased to the “Stop Output Value” which are defined at Bank0 Index08h, Index09h and Index17h.

6.5.2 Fan Speed Cruise mode

There are 4 pairs of Fan input/Fan output control at this mode: SYSFANIN with SYSFANOUT, CPUFANIN0 with CPUFANOUT0, AUXFANIN with AUXFANOUT and CPUFANIN1 with CPUFANOUT1. At this mode, W83627EHF/EHG provides the Smart Fan system which can control the fan speed automatically depend on current fan speed to keep it with in a specific range. A wanted fan speed count and interval must be set (ex. 160 ± 10) by BIOS. As long as the fan speed count is the specific range, Fan output will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), Fan output will be increased to keep the count less than the high limit. Otherwise, if current fan speed is less than the low limit(ex. 160-10), Fan output will be decreased to keep the count higher than the low limit. See Figure 6.8 example.

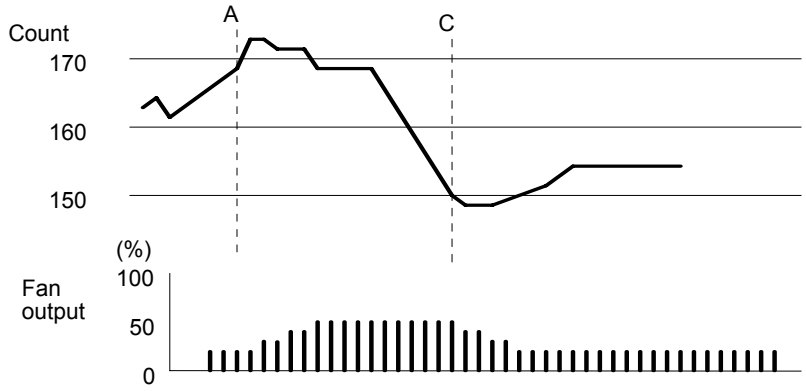


Figure 6.8

6.5.3 Manual Control Mode

Smart Fan control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software. The programming method must be set fan configuration at bank 0 index 04h,bit5-4 to 1,index 62h bit5~4 to 1. Then table 6.3-1 displayed current temperature and fan output value at Smart Fan I Mode Besides, these tables 6.3-2 and 6.3-3 used to setting thermal mode or speed cruise mode of Smart Fan I mode

Table 6.3-1 Display Register- at Smart Fan I Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 50H ,51H	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 27H	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current AUX Temperature	Bank2 50H,51H	AUXTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current CPUFANOUT0 Output Value	Bank0 03H	CPUFANOUT0 Output Value Select	FFh	Bit7-0 CPUFANOUT Value
Current SYSFANOUT Output Value	Bank0 01H	SYSFANOUT Output Value Select	FFh	Bit7-0 SYSFANOUT Value
Current AUXFANOUT Output Value	Bank0 11H	AUXFANOUT1 Output Value Select	FFh	Bit7-0 AUXFANOUT Value
Current CPUFANOUT1 Output Value	Bank0 61H	CPUFANOUT1 Output Value Select	FFh	Bit7-0 CPUFANOUT1 Value

Table 6.3-2 Relative Register-at Thermal Cruise Mode of Smart Fan I control mode

THERMAL-CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	CR[05h]	CR[07h] Bit0-3	CR[0Ah]	CR[08]h	CR[12h] Bit5	CR[0Ch]	CR[0Eh]	CR[0Fh]
CPUFANOUT0	CR[06h]	CR[07h] Bit4-7	CR[0Bh]	CR[09h]	CR[12h] Bit4	CR[0Dh]		
AUXFANOUT	CR[13h]	CR[14h] Bit0-3	CR[16h]	CR[15h]	CR[12h] Bit3	CR[17h]		
CPUFANOUT1	CR[63h]	CR[62h] Bit0-3	CR[65h]	CR[64h]	CR[12h] Bit6	CR[66h]		

Table 6.3-3 Relative Register-at Speed Cruise Mode of Smart Fan I control mode

THERMAL-CRUISE MODE	TARGET-SPEED COUNT	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	CR[05h]	CR[07h] Bit0-3	CR[12h] Bit5	CR[0Eh]	CR[0Fh]
CPUFANOUT0	CR[06h]	CR[07h] Bir4-7	CR[12h] Bir4		
AUXFANOUT0	CR[13h]	CR[14h] Bit0-3	CR[12h] Bit3		
CPUFANOUT1	CR[63h]	CR[62h] Bit0-3	CR[12h] Bit6		

SMART FAN™ III

Concept

SMART FAN™ III mode sets a target temperature through BIOS or application software and W83627EHF/EHG controls the fan speed so that the temperature could meet the target temperature set in the BIOS or software. Only Pin115 (CPUFANOUT0) and Pin120 (CPUFANOUT1) in W83627EHF/EHG support SMART FAN™ III. Pin115 (CPUFANOUT0) pairs with Pin103 (CPUTIN); while Pin120 (CPUFANOUT1) pairs with Pin104 (SYSTIN), Pin103 (CPUTIN), or Pin102 (AUXTIN), which is defined in Bank0 Index 4Ah.bit7~6.

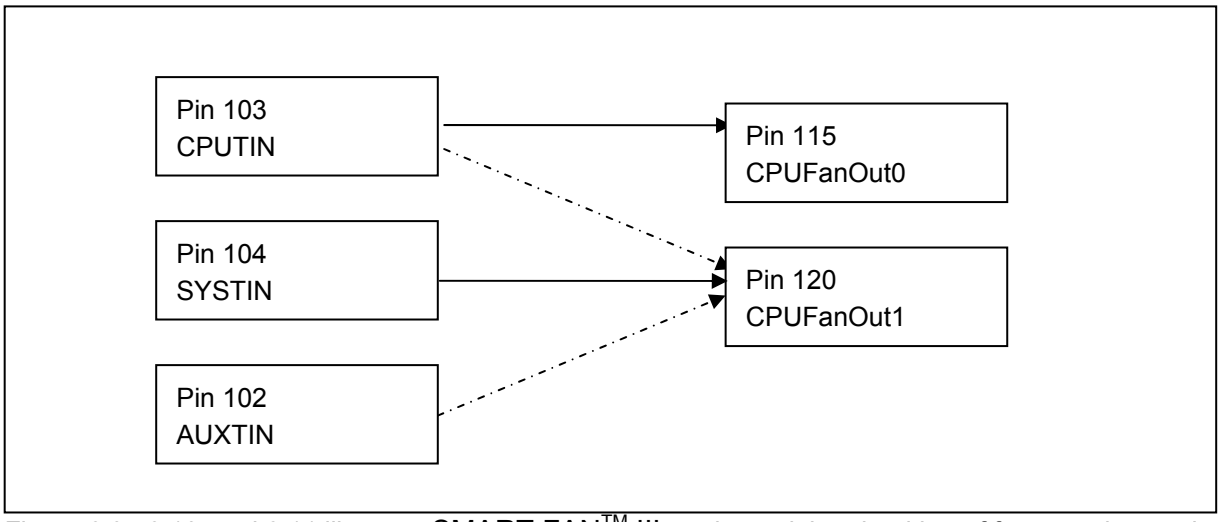


Figure 6.9, 6.10, and 6.11 illustrate SMART FAN™ III mode, and the algorithm of fan speed control is described as follows:

(1) Figure 6.9 shows the initial condition of SMART FAN™ III. Target Temperature, Temperature Tolerance, Maximum Fan Output and Minimum Fan Output must be set first. If the currently measured temperature is within the (Target Temperature ± Temperature Tolerance), the fan speed remains constant.

(2) In the case that currently measured temperature goes beyond (Target Temperature +

Temperature Tolerance), which is shown in Figure 6.10, fan speed jumps up to the next step. "Step" here refers to the value in the CPUFANOUT Output Value Select Register, Bank0 Index03h or Index61h.

(3) Meanwhile, original Target Temperature dynamically shifts to (Target Temperature + Temperature Tolerance), and new Target Temperature, named Target Temperature 1, is formed. In other words, Target Temperature 1 equals original Target Temperature plus Temperature Tolerance.

(4) If the currently measured temperature is within the (Target Temperature 1 ± Temperature Tolerance) then, the fan speed remains constant. Otherwise, fan speed jumps up to the next step again. Target Temperature then dynamically shifts to (Target Temperature 1 + Temperature Tolerance), and new Target Temperature again, named Target Temperature 2, is formed.

(5) The fan-speed-up and Target Temperature comparison-then-shift process continue until currently measured temperature locates within (Target Temperature X ± Temperature Tolerance), or fan output speed reaches its maximum speed.

(6) Please be noted that "Speed-up Slope" shown in the Figure 6.10 must be an integer. In other words, $\frac{Max.FanOutput - InitialOutput}{Steps}$ must be an integer; otherwise, it may lead to register overflow.

(7) In the case that currently measured temperature goes below (Target Temperature – Temperature Tolerance), which is shown in Figure 6.11, fan speed slows down by one step. "Step" here refers to the value in the CPUFANOUT Output Value Select Register, Bank0 Index03h or Index61h.

(8) Meanwhile, original Target Temperature dynamically shifts to (Target Temperature – Temperature Tolerance), and new Target Temperature, named Target Temperature 1, is formed. In other words, Target Temperature 1 equals original Target Temperature minus Temperature Tolerance.

(9) If the currently measured temperature is within the (Target Temperature 1 ± Temperature Tolerance) then, the fan speed remains constant. Otherwise, fan speed slows down by one step again. Target Temperature then dynamically shifts to (Target Temperature 1 – Temperature Tolerance), and new Target Temperature again, named Target Temperature 2, is formed.

(10) The fan-slow-down and Target Temperature comparison-then-shift process continue until currently measured temperature locates within (Target Temperature X ± Temperature Tolerance), or fan output speed hits its minimum speed.

(11) Please be noted that "Speed-down Slope" shown in the Figure 6.11 must be an integer. In other words, $\frac{InitialOutput - Min.FanOutput}{Step}$ must be an integer; otherwise, it may lead to register overflow.

(12) In the case that the temperature is always lower than (Target Temperature X – Temperature Tolerance), and, for some reason, the fan speed would like to be kept at the minimum speed, Stop Value, instead of being stopped, set register Bank0 12h.bit 4. Set bit 4 to 1, fan speed will always keep at the value set in Bank0 Index09h when temperature is always below (Target Temperature X – Temperature Tolerance). Set bit 4 to 0, fan speed will decrease to 0 after a time period set in Bank0 Index0Dh.

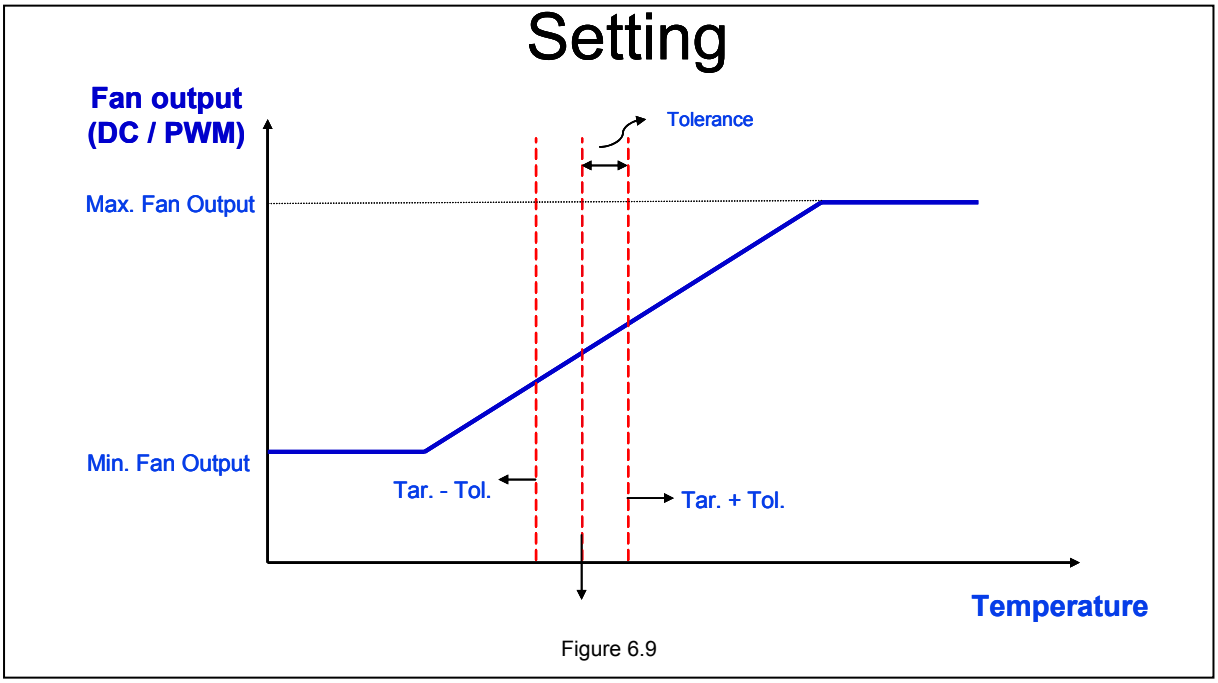


Figure 6.9

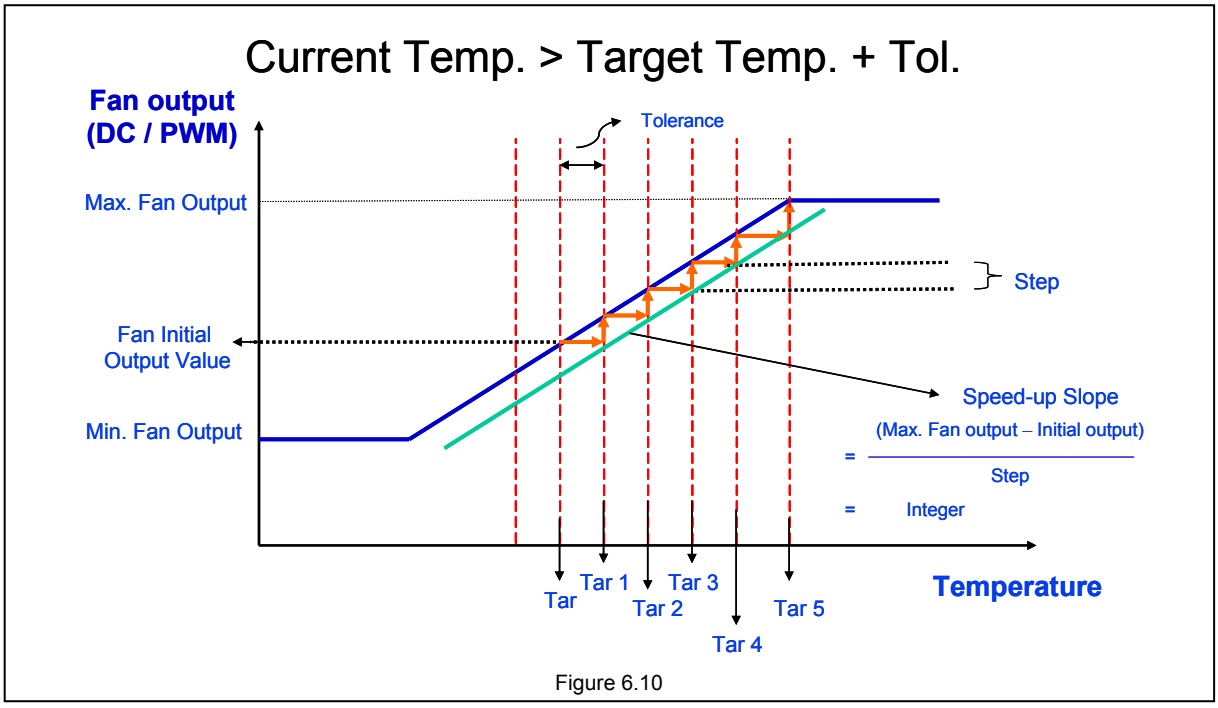


Figure 6.10

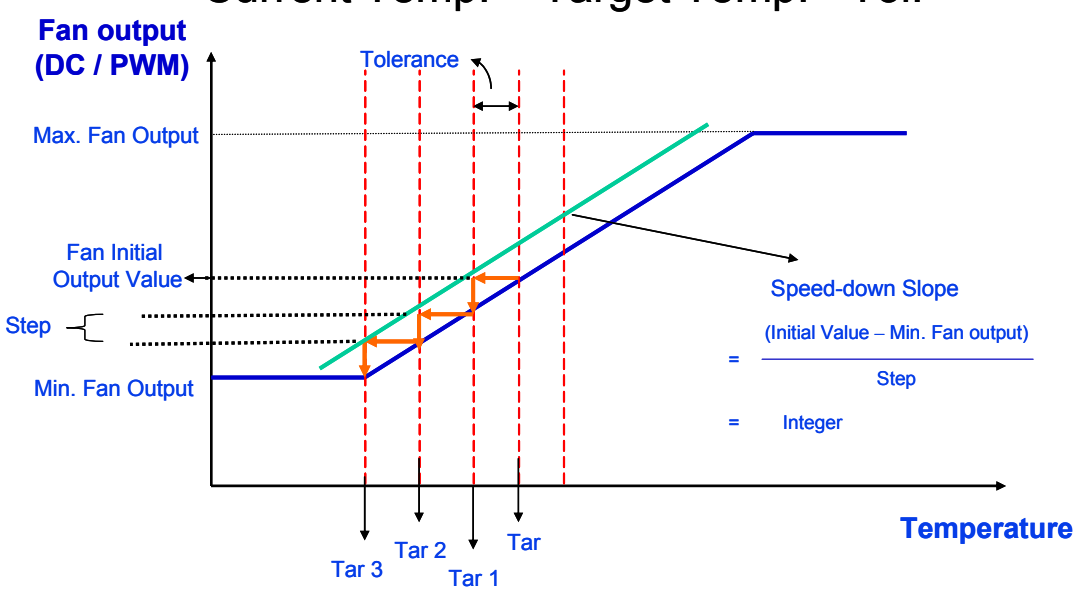


Figure 6.11

6.5.4 Smart Fan III Mode

Smart Fan III control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software. The programming method must be set fan configuration at bank 0 index 04h,bit5-4,index 12h bit2~1 index 62h bit5~4.Before enabling Smart Fan III mode ,you have to set relative registers as table 6.4-2. In addition to the required registers, the device has a the following registers that further configure and enable the fan speed control functionality .Then Table 6.4-1 displayed current temperature and fan output value at Smart Fan III mode , Besides, the table 6.4-2 used to setting at Smart Fan III mode

Table 6.4-1 Display Register- at Smart Fan III Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 50H ,51H	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 27H	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current AUX Temperature	Bank2 50H,51H	AUXTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current CPUFANOUT0 Output Value	Bank0 03H	CPUFANOUT0 Output Value Select	FFh	Bit7-0 CPUFANOUT Value
Current SYSFANOUT Output Value	Bank0 01H	SYSFANOUT Output Value Select	FFh	Bit7-0 SYSFANOUT Value

Table 6.4-2 Relative Register-at Smart Fan III control mode

SMART-FAN III MODE	TARGET TEMPERATURE	TOLERANCE	STOP VALUE (MIN. FAN OUTPUT)	MAX. FAN OUTPUT	STOP TIME
CPUFANOUT0	CR[06h]	CR[07h] bit 4-7	CR[09h]	CR[67h]	CR[0Dh]
CPUFANOUT1	CR[63h]	CR[62h] bit 0-3	CR[64h]	CR[69h]	CR[66h]
Smart-Fan III Mode	**Output Step**	**Step Down Time**	**Step Up Time**	**Keep Min. Fan Output value**	
CPUFANOUT0	CR[68h]	CR[0Eh]	CR[0Fh]	CR[12h] bit 4	
CPUFANOUT1	CR[6Ah]	CR[0Eh]	CR[0Fh]	CR[12h] bit 6	

6.6 SMI# interrupt mode

The HM_SMI#/OVT# pin is a multi-function pin. The function is selected at Configuration Register CR[29h] bit 6.

6.6.1 Voltage SMI# mode

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 6.12)

6.6.2 Fan SMI# mode

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 6.13)

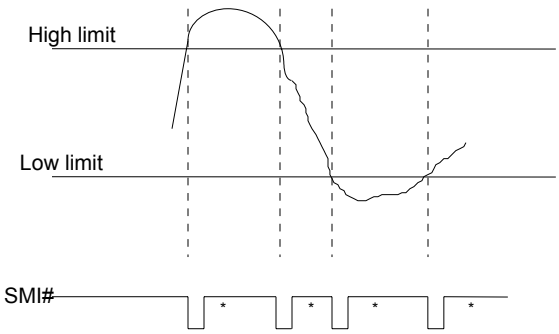


Figure 6.12

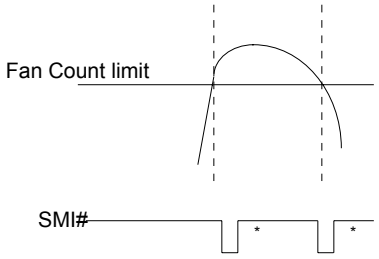


Figure 6.13

*Interrupt Reset when Interrupt Status Registers are read

6.6.3 Temperature SMI# mode

6.6.3.1. Temperature sensor 1(SYSTIN) SMI# interrupt has 3 modes

(1) Comparator Interrupt Mode

Setting the T_{HYST} (Temperature Hysteresis) limit to 127°C will set temperature sensor 1 SMI# to the Comparator Interrupt Mode. Temperature exceeds T_O (Over Temperature) Limit causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_O , the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_O. (Figure 6.14)

Setting the T_{HYST} lower than T_O will set temperature sensor 1 SMI# to the Interrupt Mode. The following are two kinds of interrupt modes, which are selected by Bank0 Index 4Ch bit5 :

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O , then reset, if the temperature remains above the T_{HYST} , the interrupt will not occur. (Figure 6.15)

(3) One-Time Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O , then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding T_O. (Figure 6.16)

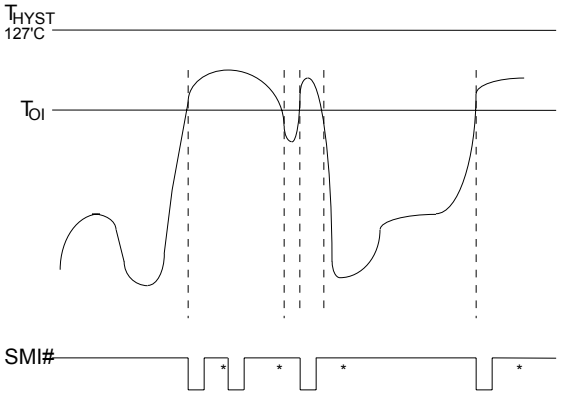


Figure 6.14

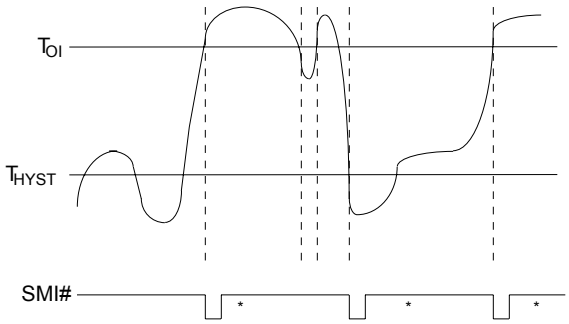
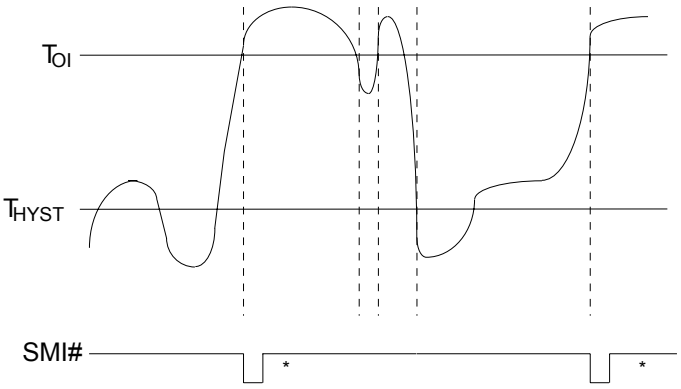


Figure 6.15

*Interrupt Reset when Interrupt Status Registers are read



*Interrupt Reset when Interrupt Status Registers are read

Figure 6.16

6.6.3.2. Temperature sensor 2(CPUTIN) and sensor 3(AUXTIN) SMI# interrupt has two modes

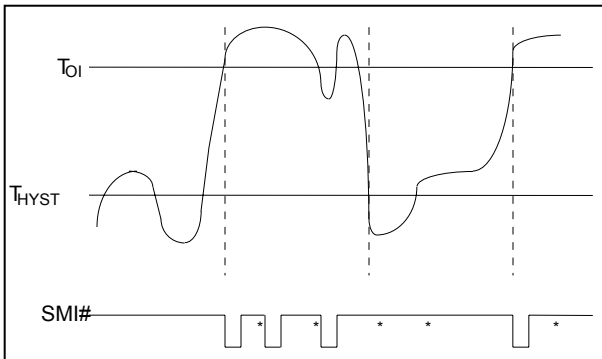
It is programmed at Bank0 Index 4Ch.bit 6.

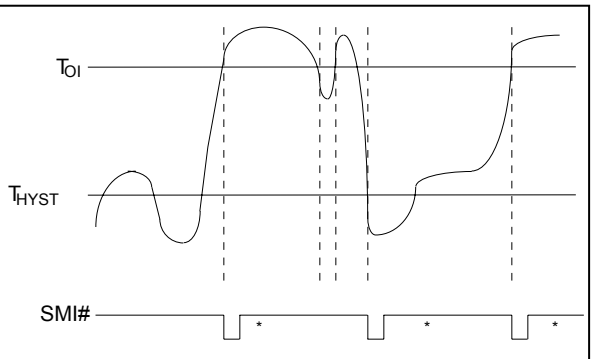
(1) Comparator Interrupt Mode

Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 6.17)

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O , then reset, if the temperature remains above the T_{HYST} , the interrupt will not occur. (Figure 6.18)





*Interrupt Reset when Interrupt Status Registers are read

Figure 6.17

Figure 6.18

6.7 OVT# interrupt mode

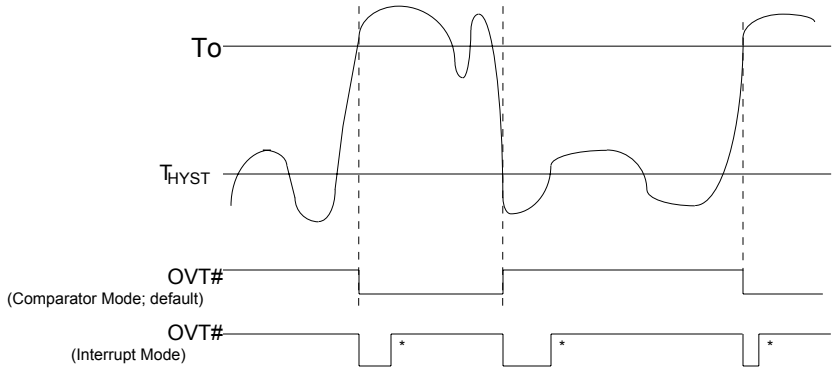
The HM_SMI#/OVT# pin (pin 5) is a multi-function pin. The function is selected at Configuration Register CR[29h] bit 6. The OVT# mode selection bits are at Bank0 Index18h bit4, Bank1 Index 52h bit1 and Bank2 Index 52h bit1.

(1) Comparator Mode :

Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 6.19)

(2) Interrupt Mode:

Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor registers. Temperature exceeding T_O , then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor registers. Once the OVT# is activated by exceeding T_O , then reset, if the temperature remains above T_{HYST} , the OVT# will not be activated again.(Figure 6.19)



*Interrupt Reset when Temperature sensor registers are read

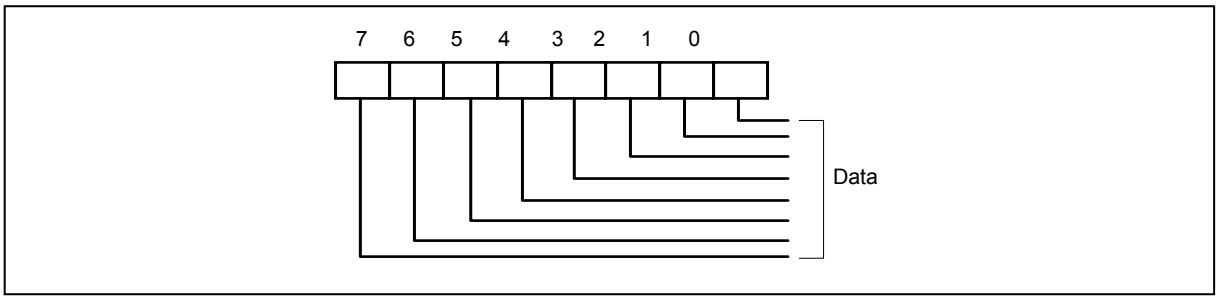
Figure 6.19

6.8 Registers and RAM

Address Port and Data Port are set in the register CR60 and CR61 of Device B which is Hardware Monitor Device. The value in CR60 is high byte and that in CR61 is low byte. For example, setting CR60 to 02 and CR61 to 90 causes the Address Port to be 0x295 and Data Port to be 0x296.

6.8.1 Address Port (Port x5h)

Address Port: Port x5h
Power on Default Value 00h
Attribute: Bit 6:0 Read/write , Bit 7: Reserved
Size: 8 bits

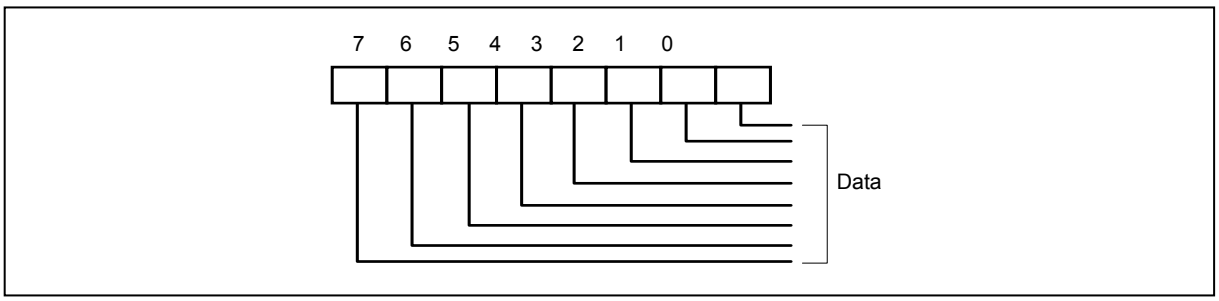


Bit7: Reserved
Bit 6-0: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Address Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

6.8.2 Data Port (Port x6h)

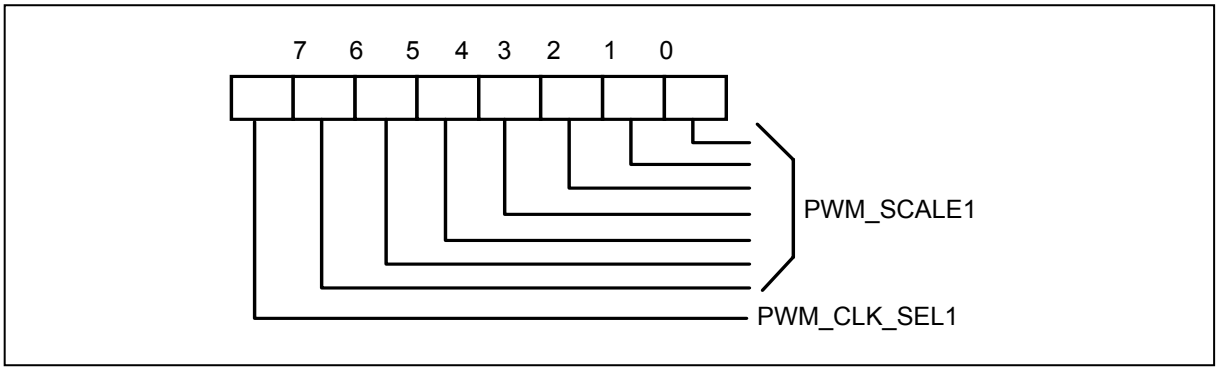
Data Port: Port x6h
Power on Default Value 00h
Attribute: Read/write
Size: 8 bits



Bit 7-0: Data to be read from or to be written to RAM and Register.

6.8.3 SYSFANOUT PWM Output Frequency Configuration Register - Index 00h (Bank 0)

Register Location: 00h
Power on Default Value: 04h
Attribute: Read/Write
Size: 8 bits



The register is meaningful when SYSFANOUT be programmed as PWM output.

Bit 7: SYSFANOUT PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

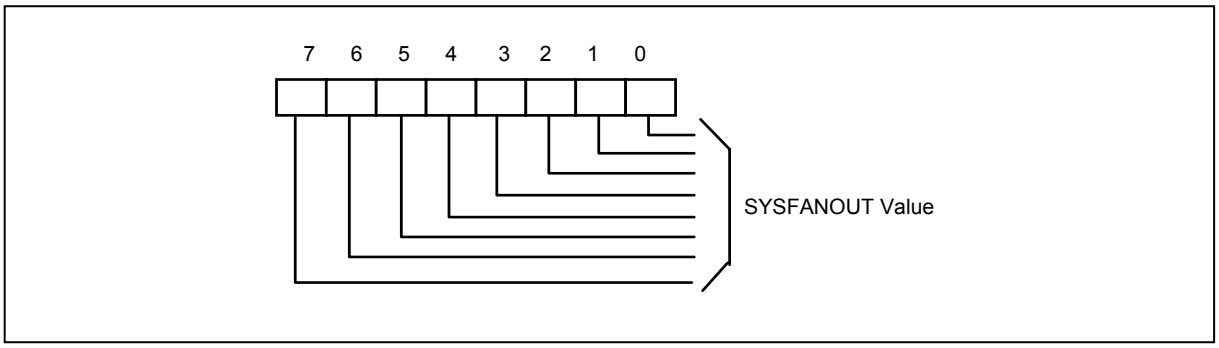
Bit 6-0: SYSFANOUT PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1
02h : divider is 2
03h : divider is 3
:
:

the formula is $$\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$$

6.8.4 SYSFANOUT Output Value Select Register - Index 01h (Bank 0)

Register Location: 01h
Power on Default Value: FFh
Attribute: Read/Write
Size: 8 bits



(1)If SYSFANOUT be programmed as PWM output (Bank0 Index 04h.bit0 is 0)

Bit 7-0: SYSFANOUT PWM Duty Cycle. Write FFh, SYSFANOUT is always logical High which means duty cycle is 100%. Write 00h, SYSFANOUT is always logical Low which means duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If SYSFANOUT be programmed as DC Voltage output (Bank0 Index 04h.bit0 is 1)

Bit 7-2: SYSFANOUT voltage control.

Bit 1-0: Reserved.

OUTPUT Voltage = $AVCC * \frac{FANOUT}{64}$

If AVCC= 3.3V , output voltage table is

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE
0	0	0	0	0	0	0	1	0	0	0	0	0	1.65
0	0	0	0	0	1	0.05	1	0	0	0	0	1	1.70
0	0	0	0	1	0	0.10	1	0	0	0	1	0	1.75
0	0	0	0	1	1	0.15	1	0	0	0	1	1	1.80
0	0	0	1	0	0	0.21	1	0	0	1	0	0	1.86
0	0	0	1	0	1	0.26	1	0	0	1	0	1	1.91
0	0	0	1	1	0	0.31	1	0	0	1	1	0	1.96
0	0	0	1	1	1	0.36	1	0	0	1	1	1	2.01
0	0	1	0	0	0	0.41	1	0	1	0	0	0	2.06
0	0	1	0	0	1	0.46	1	0	1	0	0	1	2.11
0	0	1	0	1	0	0.52	1	0	1	0	1	0	2.17
0	0	1	0	1	1	0.57	1	0	1	0	1	1	2.22
0	0	1	1	0	0	0.62	1	0	1	1	0	0	2.27
0	0	1	1	0	1	0.67	1	0	1	1	0	1	2.32
0	0	1	1	1	0	0.72	1	0	1	1	1	0	2.37
0	0	1	1	1	1	0.77	1	0	1	1	1	1	2.42
0	1	0	0	0	0	0.83	1	1	0	0	0	0	2.48
0	1	0	0	0	1	0.88	1	1	0	0	0	1	2.53
0	1	0	0	1	0	0.93	1	1	0	0	1	0	2.58
0	1	0	0	1	1	0.98	1	1	0	0	1	1	2.63
0	1	0	1	0	0	1.03	1	1	0	1	0	0	2.68
0	1	0	1	0	1	1.08	1	1	0	1	0	1	2.73
0	1	0	1	1	0	1.13	1	1	0	1	1	0	2.78
0	1	0	1	1	1	1.19	1	1	0	1	1	1	2.84
0	1	1	0	0	0	1.24	1	1	1	0	0	0	2.89

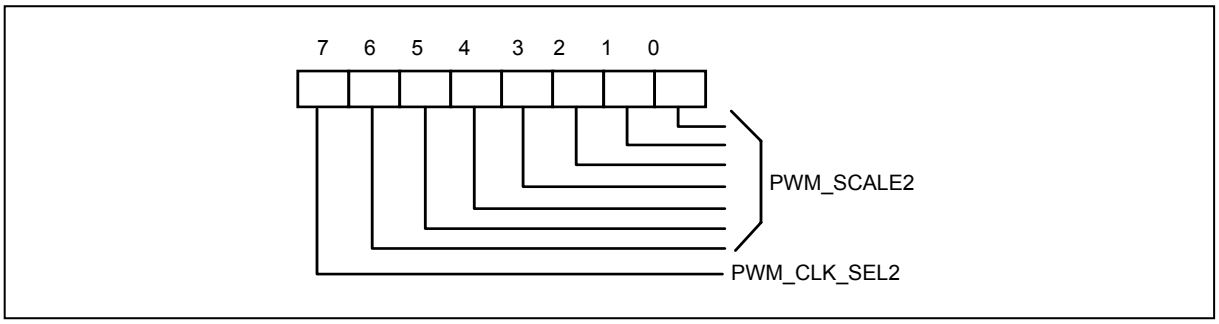
Continued.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE
0	1	1	0	0	1	1.29	1	1	1	0	0	1	2.94
0	1	1	0	1	0	1.34	1	1	1	0	1	0	2.99
0	1	1	0	1	1	1.39	1	1	1	0	1	1	3.04
0	1	1	1	0	0	1.44	1	1	1	1	0	0	3.09
0	1	1	1	0	1	1.50	1	1	1	1	0	1	3.15
0	1	1	1	1	0	1.55	1	1	1	1	1	0	3.20
0	1	1	1	1	1	1.60	1	1	1	1	1	1	3.25

Table 6.4 .

6.8.5 CPUFANOUT0 PWM Output Frequency Configuration Register - Index 02h (Bank 0)

Register Location: 02h
Power on Default Value: 04h
Attribute: Read/Write
Size: 8 bits



The register is meaningful when CPUFANOUT0 be programmed as PWM output.

Bit 7: CPUFANOUT0 PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

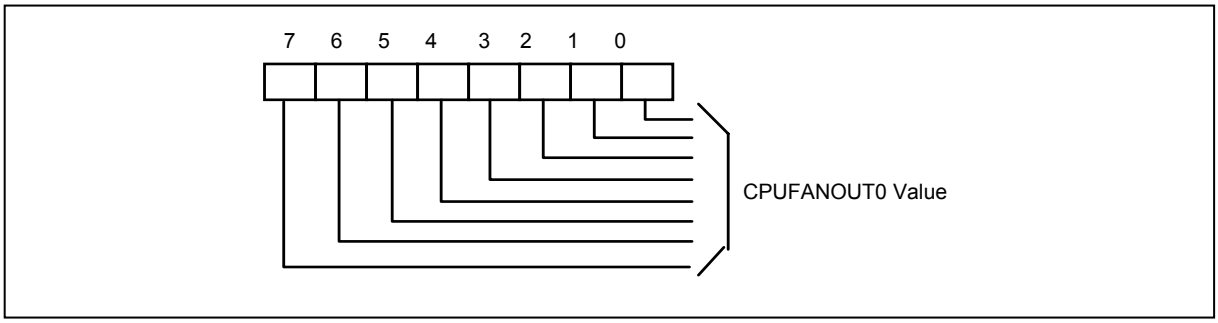
Bit 6-0: CPUFANOUT0 PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1
02h : divider is 2
03h : divider is 3
:
:

the formula is **PWM output frequency =** $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$

6.8.6 CPUFANOUT0 Output Value Select Register - Index 03h (Bank 0)

Register Location: 03h
Power on Default Value: FFh
Attribute: Read/Write
Size: 8 bits



(1)If CPUFANOUT0 be programmed as PWM output (Bank0 Index 04h.bit1 is 0)

Bit 7-0: CPUFANOUT0 PWM Duty Cycle. Write FFh, CPUFANOUT0 duty cycle is 100%. Write 00h, CPUFANOUT duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If CPUFANOUT0 be programmed as DC Voltage output (Bank0 Index 04h.bit1 is 1)

Bit 7-2: CPUFANOUT0 voltage control.

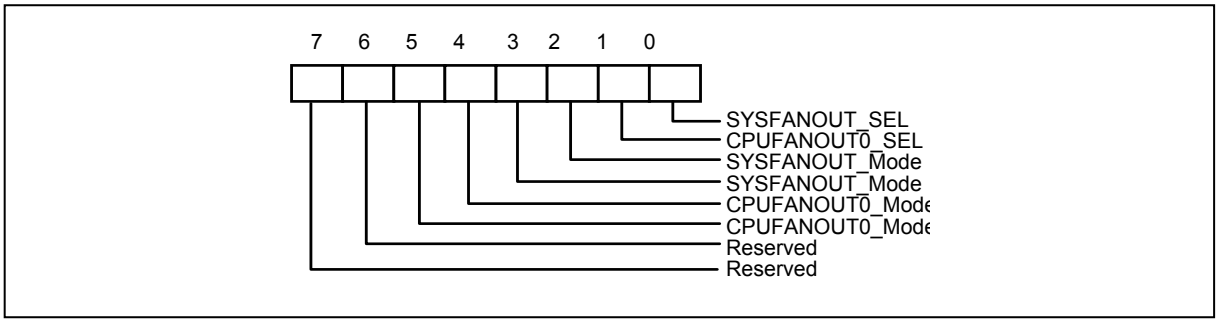
Bit 1-0: Reserved.

OUTPUT Voltage = $AVCC * \frac{FANOUT}{64}$

Note. See the Table 6.4

6.8.7 FAN Configuration Register I - Index 04h (Bank 0)

Register Location: 04h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits



Bit 7-6: Reserved

Bit 5-4: CPUFANOUT0 mode control.

Set 00, CPUFANOUT0 is as Manual Mode. (Default).
Set 01, CPUFANOUT0 is as Thermal Cruise Mode.
Set 10, CPUFANOUT0 is as Fan Speed Cruise Mode.
Set 11, CPUFANOUT0 is as SMART FAN™ III Mode

Bit 3-2: SYSFANOUT mode control.

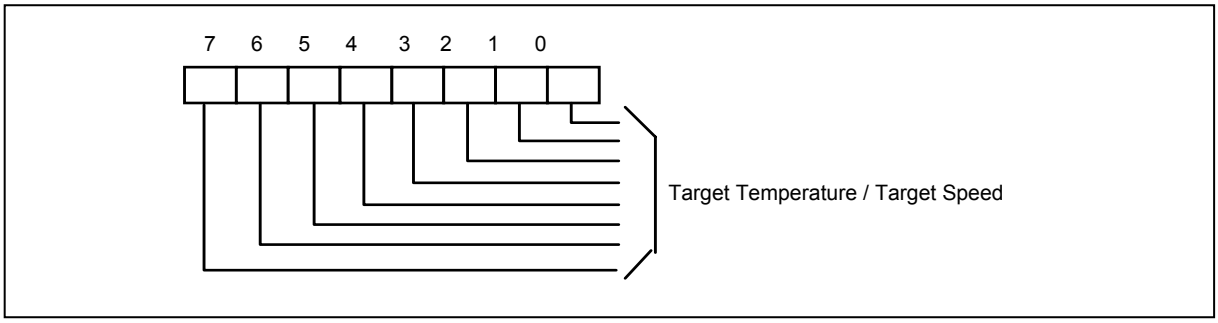
Set 00, SYSFANOUT is as Manual Mode. (Default).
Set 01, SYSFANOUT is as Thermal Cruise Mode.
Set 10, SYSFANOUT is as Fan Speed Cruise Mode.
Set 11, reserved and no function..

Bit 1: CPUFANOUT0 output mode selection. Set to 0, CPUFANOUT0 pin is as PWM output duty cycle so that it can drive a logical high or low signal. Set to 1, CPUFANOUT0 pin is as DC voltage output which can provide analog voltage output . (Default 0)

Bit 0: SYSFANOUT output mode selection. Set to 0, SYSFANOUT pin is as PWM duty cycle output so that it can drive a logical high or low signal. Set to 1, SYSFANOUT pin is as DC voltage output which can provide analog voltage output . (Default 1)

6.8.8 SYSTIN Target Temperature Register/ SYSFANIN Target Speed Register - Index 05h (Bank 0)

Register Location: 05h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits

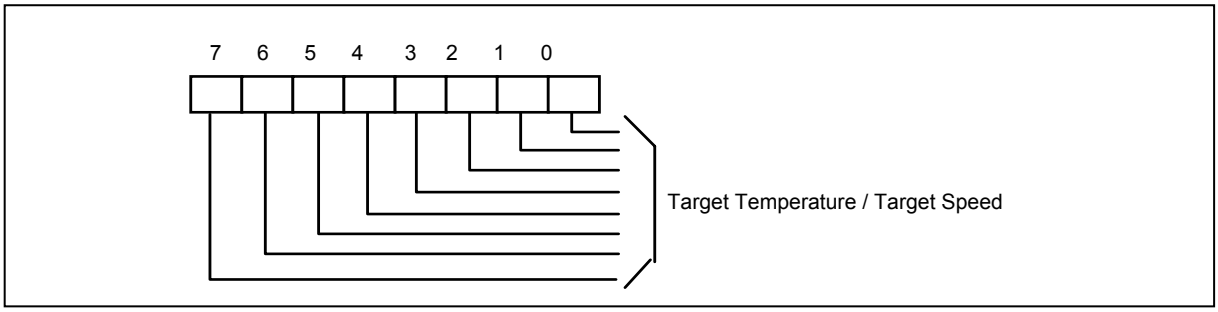


(1)When at Thermal Cruise mode:
Bit 7: Reserved.
Bit 6-0: SYSTIN Target Temperature.

(2)When at Fan Speed Cruise mode:
Bit 7-0: SYSFANIN Target Speed.

6.8.9 CPUTIN Target Temperature Register/ CPUFANIN0 Target Speed Register - Index 06h (Bank 0)

Register Location:	06h
Power on Default Value:	00h
Attribute:	Read/Write
Size:	8 bits

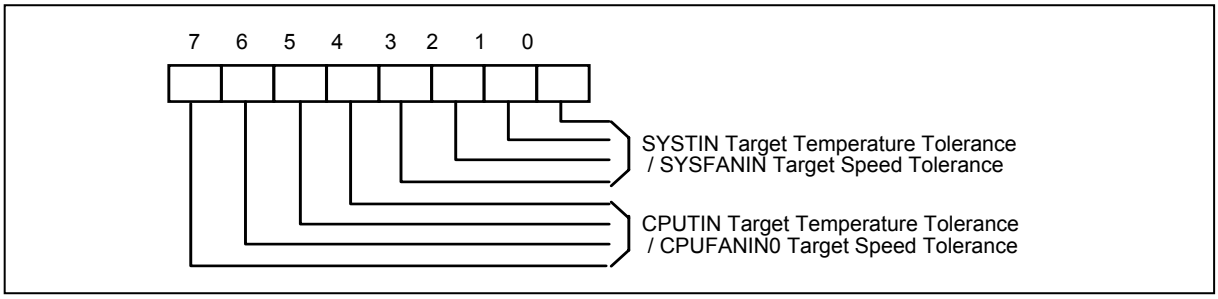


(1)When at Thermal Cruise mode or SMARTFAN III mode:
Bit 7: Reserved.
Bit 6-0: CPUTIN Target Temperature.

(2)When at Fan Speed Cruise mode:
Bit 7-0: CPUFANIN0 Target Speed.

6.8.10 Tolerance of Target Temperature or Target Speed Register - Index 07h (Bank 0)

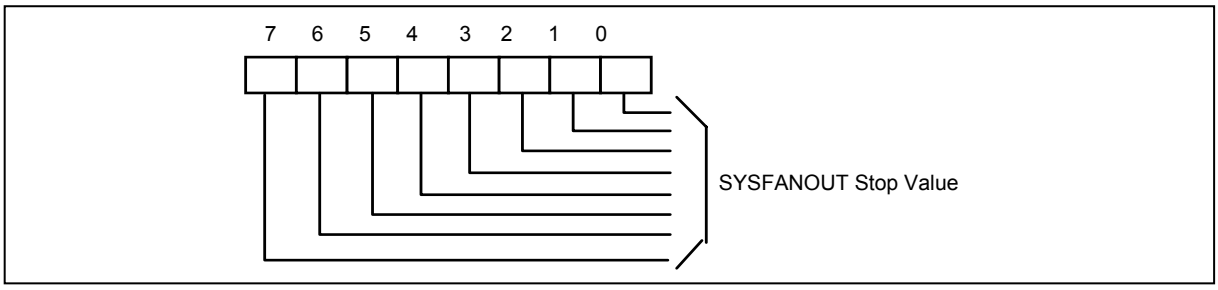
Register Location: 07h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



(1)When at Thermal Cruise mode or SMARTFAN III mode:
Bit 7-4: Tolerance of CPUTIN Target Temperature.
Bit 3-0: Tolerance of SYSTIN Target Temperature.
(2)When at Fan Speed Cruise mode:
Bit 7-4: Tolerance of CPUFANIN0 Target Speed.
Bit 3-0: Tolerance of SYSFANIN Target Speed.

6.8.11 SYSFANOUT Stop Value Register - Index 08h (Bank 0)

Register Location: 08h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits

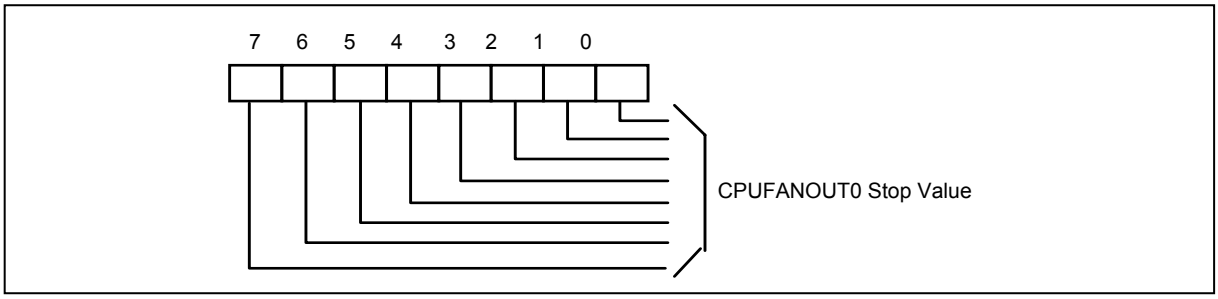


When at Thermal Cruise mode, SYSFANOUT value will decrease to this value. This register should be written a non-zero minimum stop value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

6.8.12 CPUFANOUT0 Stop Value Register - Index 09h (Bank 0)

Register Location: 09h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits

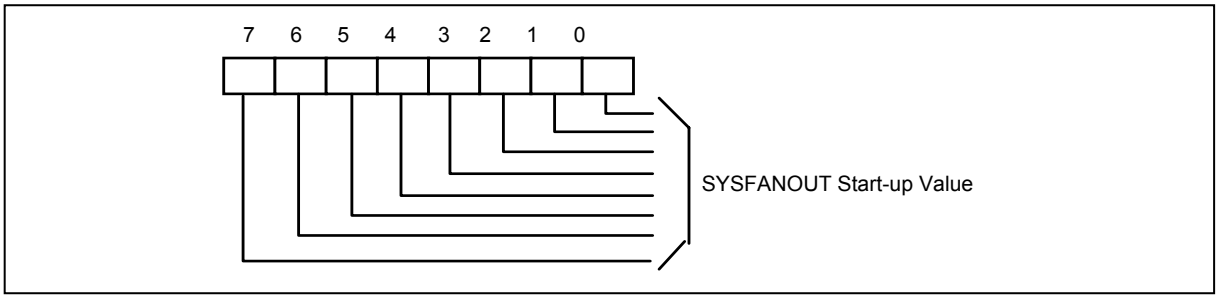


When at Thermal Cruise mode or SMARTFAN III mode, CPUFANOUT0 value will decrease to this value. This register should be written a non-zero minimum stop value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

6.8.13 SYSFANOUT Start-up Value Register - Index 0Ah (Bank 0)

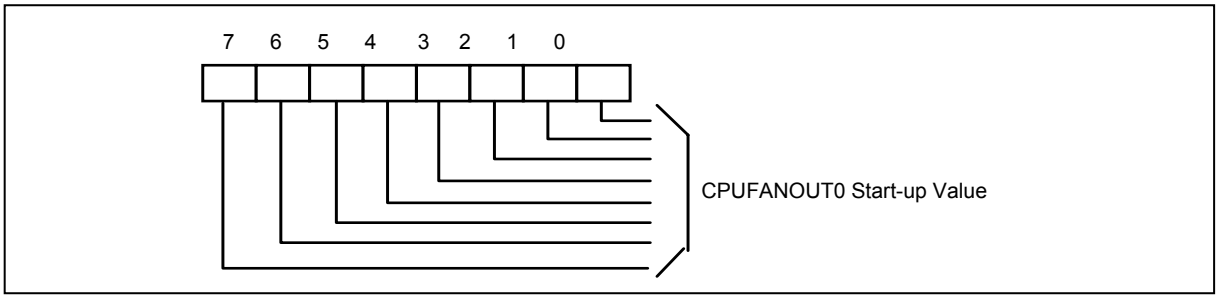
Register Location: 0Ah
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, SYSFANOUT value will increase from 0 to this register value to provide a minimum value to turn on the fan.

6.8.14 CPUFANOUT0 Start-up Value Register - Index 0Bh (Bank 0)

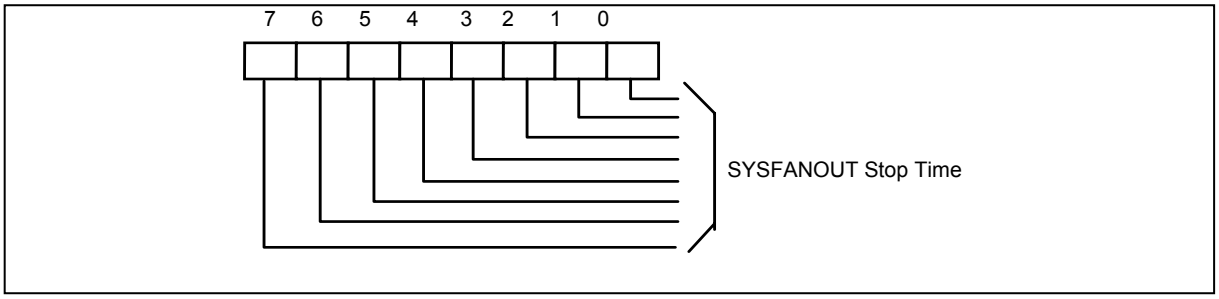
Register Location: 0Bh
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, CPUFANOUT0 value will increase from 0 to this register value to provide a minimum value to turn on the fan.

6.8.15 SYSFANOUT Stop Time Register - Index 0Ch (Bank 0)

Register Location: 0Ch
Power on Default Value: 3Ch
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, this register determines the time of which SYSFANOUT value is from stop value to 0.

(1)When at PWM output:

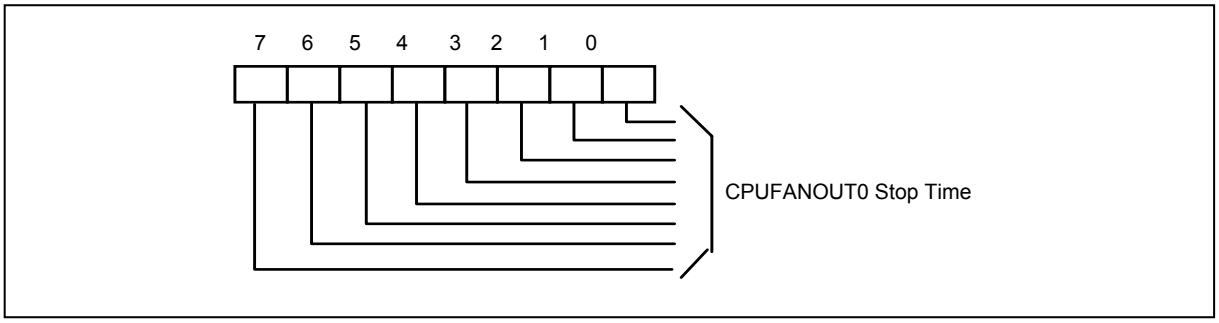
The unit of this register is 0.1 second. The default time is 6 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 24 seconds.

6.8.16 CPUFANOUT0 Stop Time Register - Index 0Dh (Bank 0)

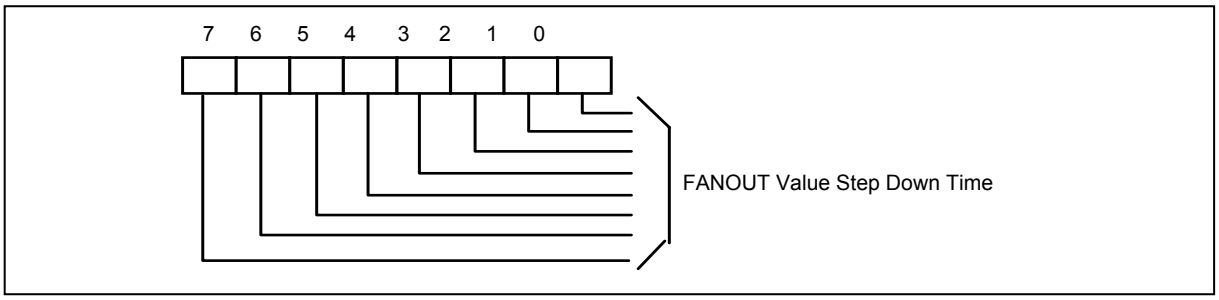
Register Location: 0Dh
Power on Default Value: 3Ch
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode or SMARTFAN III mode, this register determines the time of which CPUFANOUT0 value is from stop value to 0.
(1)When at PWM output:
The unit of this register is 0.1 second. The default time is 6 seconds.
(2)When at DC Voltage output:
The unit of this register is 0.4 second. The default time is 24 seconds.

6.8.17 Fan Output Step Down Time Register - Index 0Eh (Bank 0)

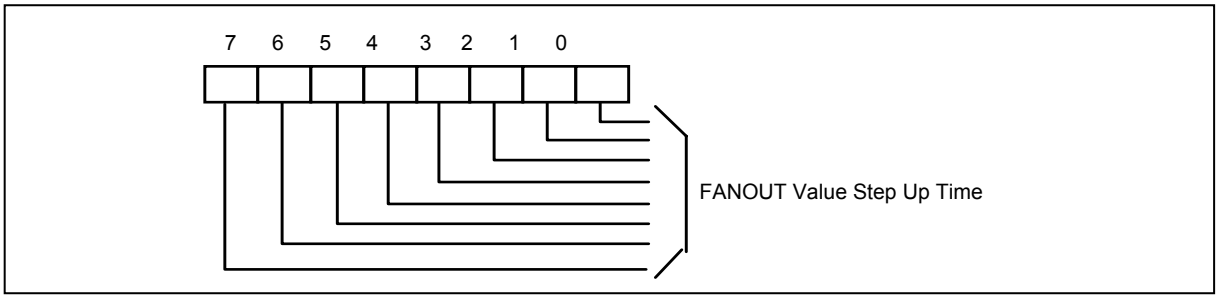
Register Location: 0Eh
Power on Default Value: 0Ah
Attribute: Read/Write
Size: 8 bits



This register determines the speed of FANOUT decreasing its value in Smart Fan Control mode.
(1)When at PWM output:
The unit of this register is 0.1 second. The default time is 1 seconds.
(2)When at DC Voltage output:
The unit of this register is 0.4 second. The default time is 4 seconds.

6.8.18 Fan Output Step Up Time Register - Index 0Fh (Bank 0)

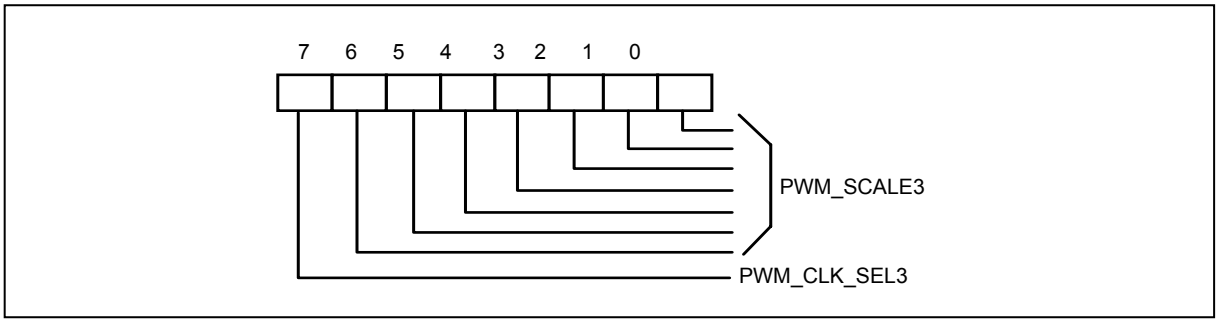
Register Location: 0Fh
Power on Default Value: 0Ah
Attribute: Read/Write
Size: 8 bits



This register determines the speed of FANOUT increasing the its value in Smart Fan Control mode.
(1)When at PWM output:
The unit of this register is 0.1 second. The default time is 1 seconds.
(2)When at DC Voltage output:
The unit of this register is 0.4 second. The default time is 4 seconds.

6.8.19 AUXFANOUT PWM Output Frequency Configuration Register - Index 10h (Bank 0)

Register Location: 10h
Power on Default Value: 04h
Attribute: Read/Write
Size: 8 bits



The register is meaningful when AUXFANOUT be programmed as PWM output.

Bit 7: AUXFANOUT PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.
Set to 0, select 24 MHz.
Set to 1, select 180 KHz.

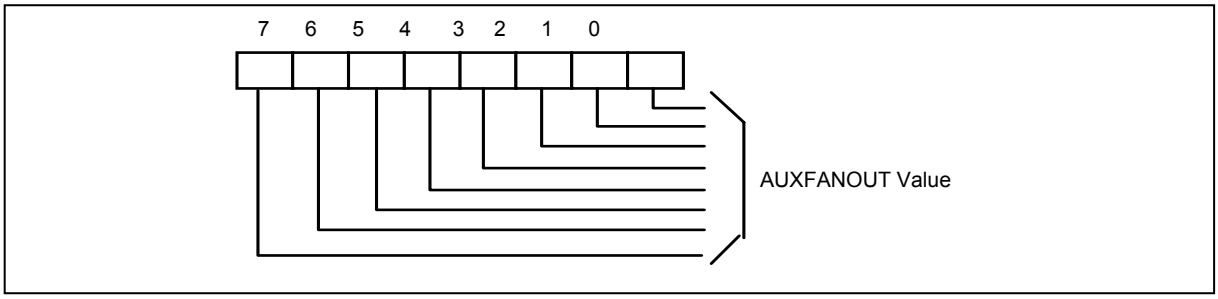
Bit 6-0: AUXFANOUT PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1
02h : divider is 2
03h : divider is 3
:
:

the formula is **PWM output frequency =** $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$

6.8.20 AUXFANOUT Output Value Select Register - Index 11h (Bank 0)

Register Location: 11h
Power on Default Value: FFh
Attribute: Read/Write
Size: 8 bits



(1)If AUXFANOUT be programmed as PWM output (Bank0 Index 12h.bit0 is 0)

Bit 7-0: AUXFANOUT PWM Duty Cycle. Write FFh, AUXFANOUT duty cycle is 100%. Write 00h, AUXFANOUT duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If AUXFANOUT be programmed as DC Voltage output (Bank0 Index 12h.bit0 is 1)

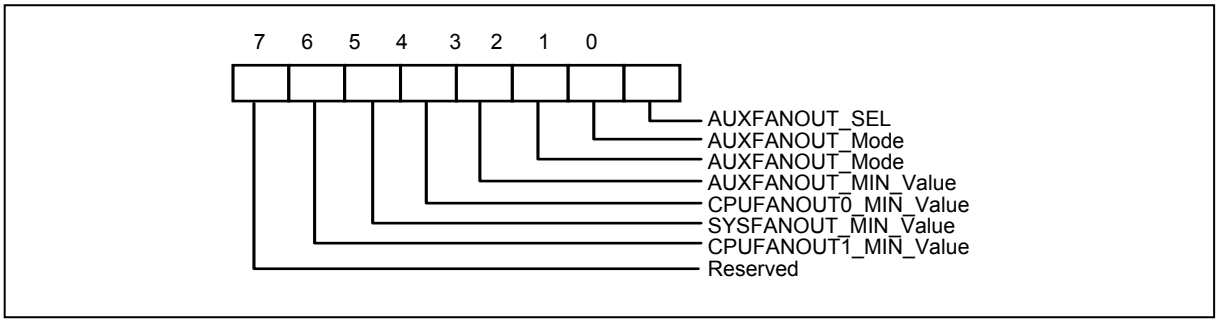
Bit 7-2: AUXFANOUT voltage control.
Bit 1-0: Reserved.

OUTPUT Voltage = $AVCC * \frac{FANOUT}{16}$

Note. See the Table 6.4

6.8.21 FAN Configuration Register II - Index 12h (Bank 0)

Register Location: 12h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Reserved

Bit 6: Set 1, CPUFANOUT1 value will decrease to and keep the value set in Index 64h when temperature goes below target range. This is to maintain the fan speed in a minimum value.
Set 0, CPUFANOUT1 value will decrease to 0 when temperature goes below target range.

Bit 5: Set 1, SYSFANOUT value will decrease to and keep the value set in Index 08h when temperature goes below target range. This is to maintain the fan speed in a minimum value.
Set 0, SYSFANOUT value will decrease to 0 when temperature goes below target range.

Bit 4: Set 1, CPUFANOUT0 value will decrease to and keep the value set in Index 09h when temperature goes below target range. This is to maintain the fan speed in a minimum value.
Set 0, CPUFANOUT0 value will decrease to 0 when temperature goes below target range.

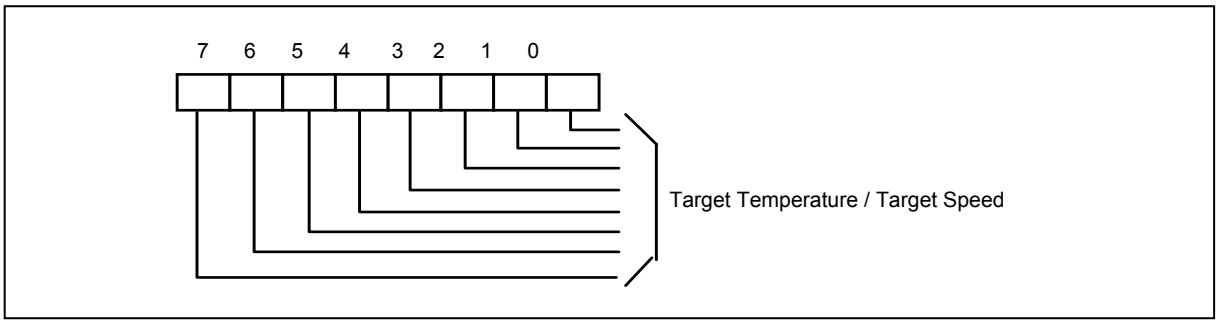
Bit 3: Set 1, AUXFANOUT value will decrease to and keep the value set in Index 17h when temperature goes below target range. This is to maintain the fan speed in a minimum value.
Set 0, AUXFANOUT value will decrease to 0 when temperature goes below target range.

Bit 2-1: AUXFANOUT mode control.
Set 00, AUXFANOUT is as Manual Mode. (Default).
Set 01, AUXFANOUT is as Thermal Cruise Mode.
Set 10, AUXFANOUT is as Fan Speed Cruise Mode.
Set 11, reserved and no function.

Bit 0: AUXFANOUT output mode selection. Set to 0, AUXFANOUT pin is as PWM output duty cycle so that it can drive a logical high or low signal. Set to 1, AUXFANOUT pin is as DC voltage output which can provide analog voltage output. (Default 0)

6.8.22 AUXTIN Target Temperature Register/ AUXFANIN0 Target Speed Register - Index 13h (Bank 0)

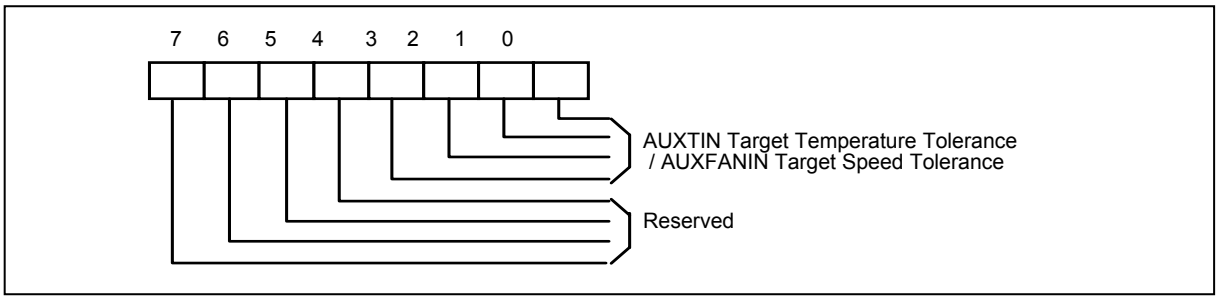
Register Location: 13h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



(1)When at Thermal Cruise mode:
Bit 7: Reserved.
Bit 6-0: AUXTIN Target Temperature.
(2)When at Fan Speed Cruise mode:
Bit 7-0: AUXFANIN0 Target Speed.

6.8.23 Tolerance of Target Temperature or Target Speed Register - Index 14h (Bank 0)

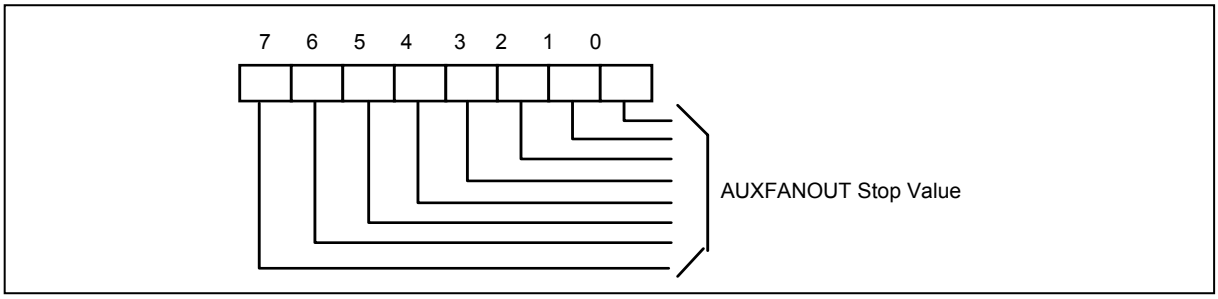
Register Location: 14h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



(1)When at Thermal Cruise mode:
Bit 3-0: Tolerance of AUXTIN Target Temperature.
(2)When at Fan Speed Cruise mode:
Bit 3-0: Tolerance of AUXFANIN0 Target Speed.

6.8.24 AUXFANOUT Stop Value Register - Index 15h (Bank 0)

Register Location: 15h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits

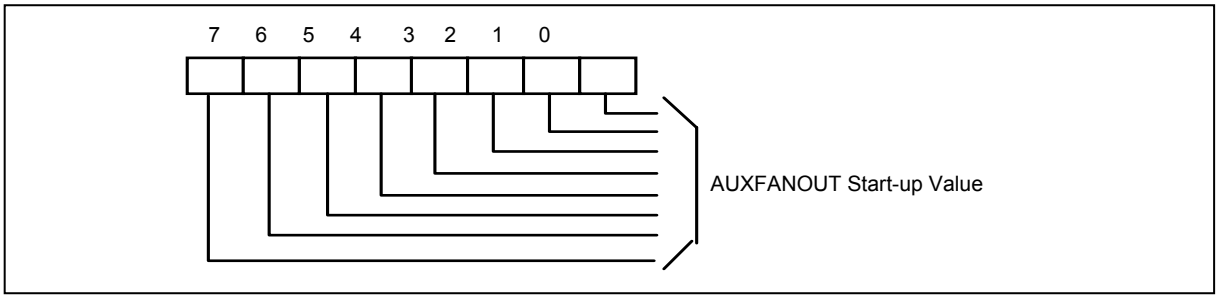


When at Thermal Cruise mode, AUXFANOUT value will decrease to this value. This register should be written a non-zero minimum output value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

6.8.25 AUXFANOUT Start-up Value Register - Index 16h (Bank 0)

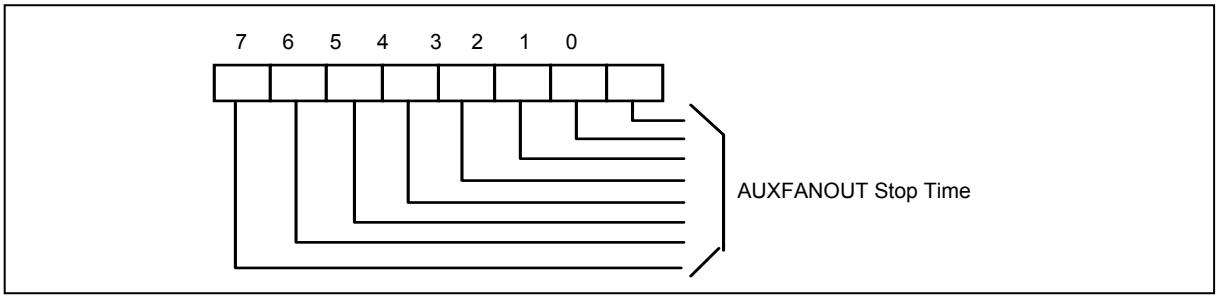
Register Location: 16h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, AUXFANOUT value will increase from 0 to this register value to provide a minimum value to turn on the fan.

6.8.26 AUXFANOUT Stop Time Register - Index 17h (Bank 0)

Register Location: 17h
Power on Default Value: 3Ch
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, this register determines the time of which AUXFANOUT value is from stop value to 0.

(1)When at PWM output:

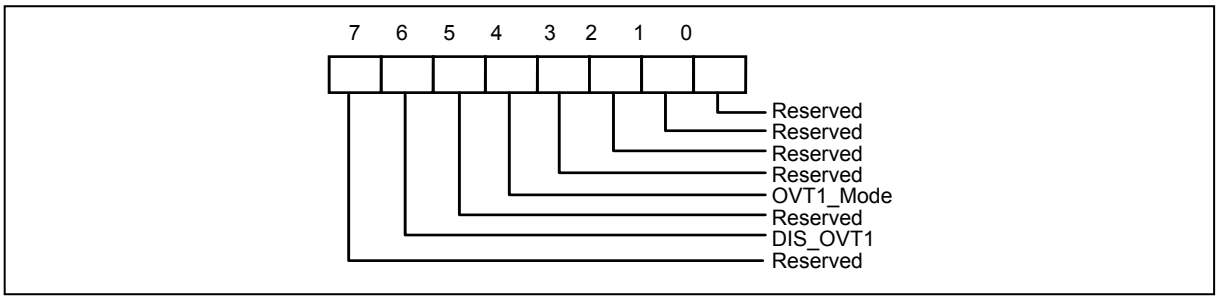
The unit of this register is 0.1 second. The default time is 6 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 24 seconds.

6.8.27 OVT# Configuration Register - Index 18h (Bank 0)

Register Location: 18h
Power on Default Value: 43h
Attribute: Read/Write
Size: 8 bits



Bit 7: Reserved.

Bit 6: Set to 1, disable temperature sensor SYSTIN over-temperature (OVT#) output. Set to 0, enable the SYSTIN OVT# output.

Bit 5: Reserved.

Bit 4: SYSTIN OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 3-1: Reserved.

Bit 0: Reserved.

6.8.28 Reserved - Index 19h (Bank 0)

6.8.29 Reserved - Index 1A-1Bh (Bank 0)

6.8.30 Reserved - Index 1Ch-1Fh (Bank 0)

6.8.31 Value RAM — Index 20h- 3Fh (Bank 0)

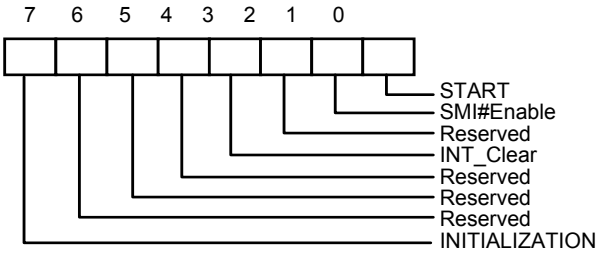
ADDRESS A6-A0	DESCRIPTION
20h	CPUVCORE reading
21h	VIN0 reading
22h	AVCC reading
23h	3VCC reading
24h	VIN1 reading
25h	VIN2 reading
26h	VIN3 reading
27h	SYSTIN temperature sensor reading
28h	SYSFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
29h	CPUFANIN0 reading Note: This location stores the number of counts of the internal clock per revolution.
2Ah	AUXFANIN0 reading Note: This location stores the number of counts of the internal clock per revolution.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN0 High Limit
2Eh	VIN0 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN1 High Limit
34h	VIN1 Low Limit
35h	VIN2 High Limit
36h	VIN2 Low Limit

Continued.

ADDRESS A6-A0	DESCRIPTION
37h	VIN3 High Limit
38h	VIN3 Low Limit
39h	SYSTIN temperature sensor High Limit
3Ah	SYSTIN temperature sensor Hysteresis Limit
3Bh	SYSFANIN Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	CPUFANIN0 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	AUXFANIN0 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Eh	CPUFANIN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Fh	CPUFANIN1 reading Note: This location stores the number of counts of the internal clock per revolution.

6.8.32 Configuration Register - Index 40h (Bank 0)

Register Location: 40h
Power on Default Value: 03h
Attribute: Read/Write
Size: 8 bits



Bit 7: A one restores power on default value to some registers. This bit clears itself since the power on default is zero.
Bit 6: Reserved
Bit 5: Reserved

Bit 4: Reserved

Bit 3: A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: Reserved

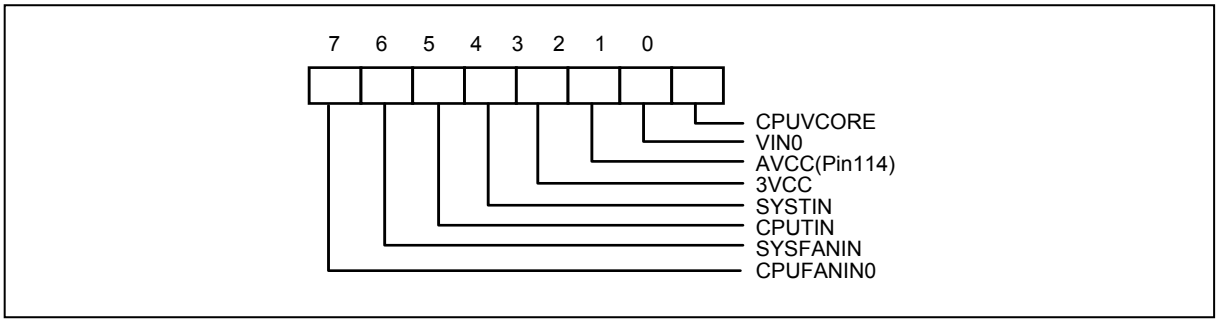
Bit 1: A one enables the SMI# Interrupt output.

Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

6.8.33 Interrupt Status Register 1 - Index 41h (Bank 0)

Register Location: 41h
Power on Default Value: 00h
Attribute: Read Only
Size: 8 bits



Bit 7: A one indicates the fan count limit of CPUFANIN0 has been exceeded.

Bit 6: A one indicates the fan count limit of SYSFANIN has been exceeded.

Bit 5: A one indicates a High limit of CPUTIN temperature has been exceeded.

Bit 4: A one indicates a High limit of SYSTIN temperature has been exceeded .

Bit 3: A one indicates a High or Low limit of 3VCC has been exceeded.

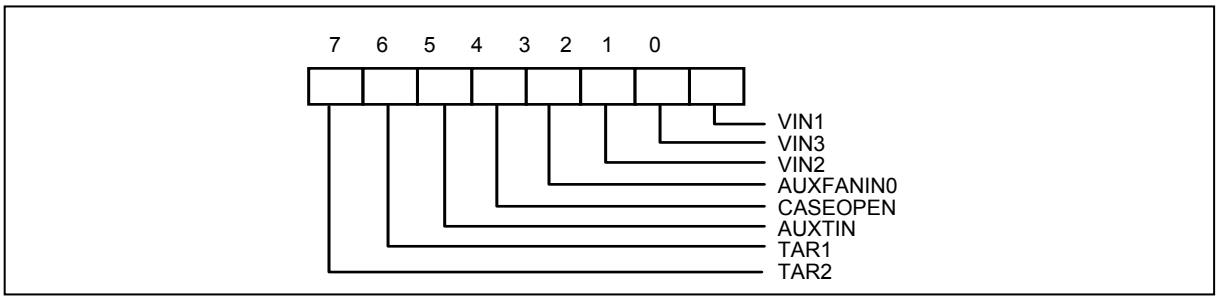
Bit 2: A one indicates a High or Low limit of AVCC has been exceeded.

Bit 1: A one indicates a High or Low limit of VIN0 has been exceeded.

Bit 0: A one indicates a High or Low limit of CPUVCORE has been exceeded.

6.8.34 Interrupt Status Register 2 - Index 42h (Bank 0)

Register Location: 42h
Power on Default Value: 00h
Attribute: Read Only
Size: 8 bits



Bit 7: A one indicates that the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 6: A one indicates that the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 5: A one indicates a High limit of AUXTIN temperature has been exceeded.

Bit 4: A one indicates case has been opened.

Bit 3: A one indicates the fan count limit of AUXFANIN0 has been exceeded .

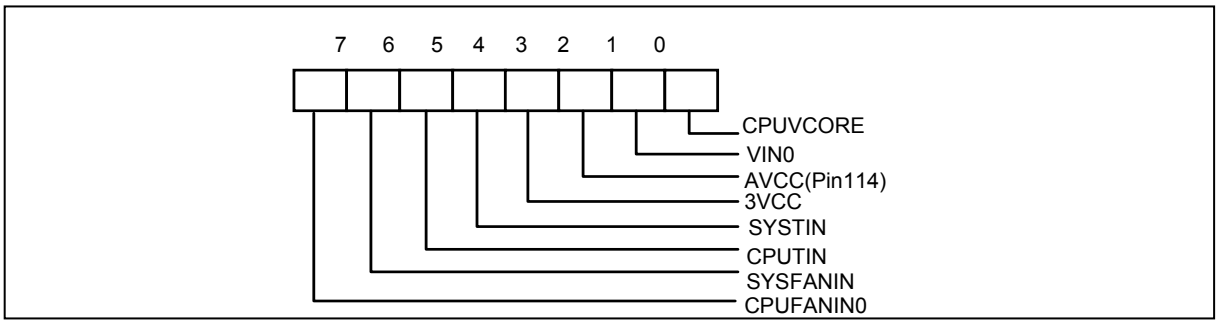
Bit 2: A one indicates a High or Low limit of VIN2 has been exceeded.

Bit 1: A one indicates a High or Low limit of VIN3 has been exceeded.

Bit 0: A one indicates a High or Low limit of VIN1 has been exceeded.

6.8.35 SMI# Mask Register 1 - Index 43h (Bank 0)

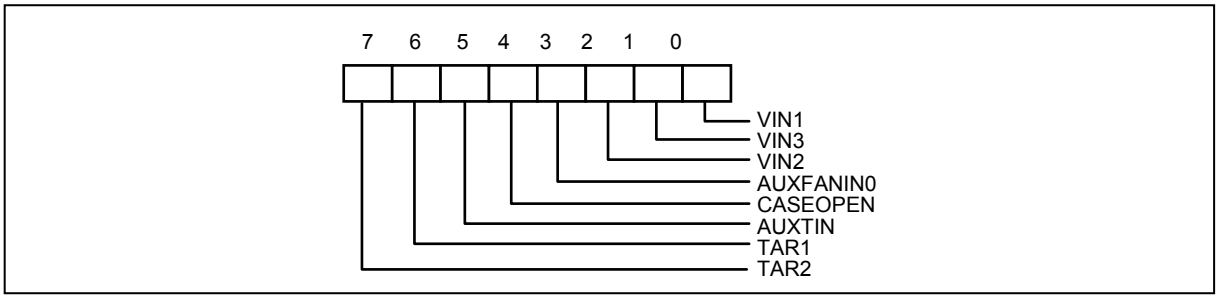
Register Location: 43h
Power on Default Value: DEh
Attribute: Read/Write
Size: 8 bits



Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

6.8.36 SMI# Mask Register 2 - Index 44h (Bank 0)

Register Location: 44h
Power on Default Value: FFh
Attribute: Read/Write
Size: 8 bits

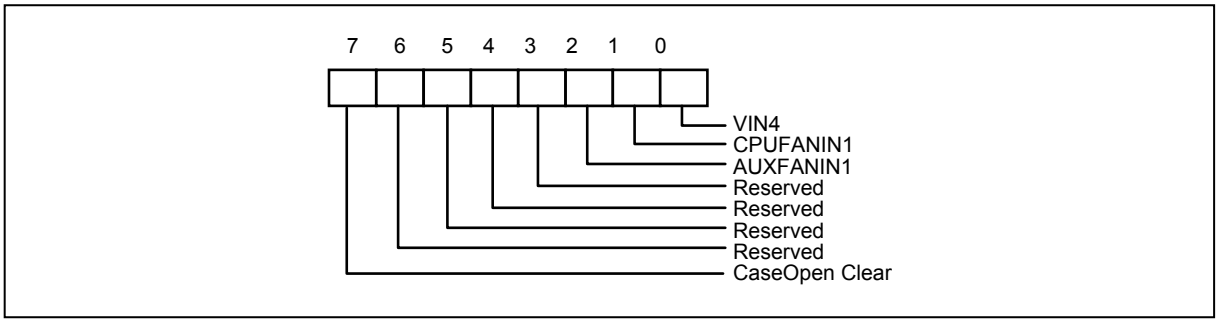


Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

6.8.37 Reserved Register - Index 45h (Bank 0)

6.8.38 SMI# Mask Register 3 - Index 46h (Bank 0)

Register Location: 46h
Power on Default Value: 07h
Attribute: Read/Write
Size: 8 bits



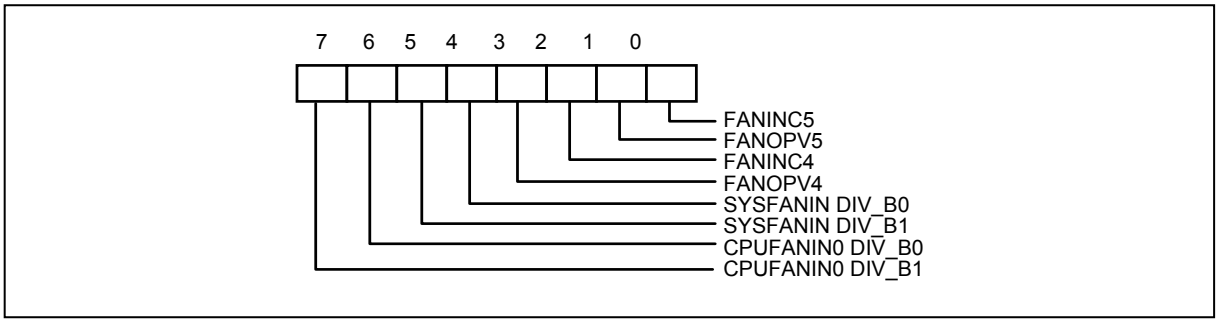
Bit 7: CASEOPEN Clear Control. Write 1 to this bit will clear CASEOPEN status. This bit won't be self cleared, please write 0 after event be cleared. The function is as same as LDA, CR[E6h] bit 5.

Bit 6-3: Reserved.

Bit 2-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

6.8.39 Fan Divisor Register I - Index 47h (Bank 0)

Register Location: 47h
Power on Default Value: 55h
Attribute: Read/Write
Size: 8 bits



Bit 7-6: CPUFANIN0 Divisor bit1:0.

Bit 5-4: SYSFANIN Divisor bit1:0.

Bit 3: CPUFANIN1 output value if bit 0 sets to 0. Write 1, pin119(CPUFANIN1) always generates a logic high signal. Write 0, pin119 always generates a logic low signal. This bit is default 0.

Bit 2: CPUFANIN1 Input Control. Set to 1, pin119 (CPUFANIN1) acts as FAN tachometer input, which is default value. Set to 0, this pin119 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

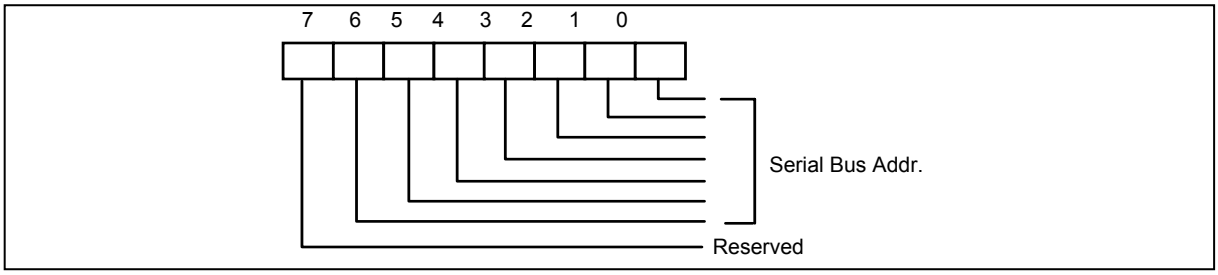
Bit 1: AUXFANIN1 output value if bit 0 sets to 0. Write 1, pin58(AUXFANIN1) always generates a logic high signal. Write 0, pin58 always generates a logic low signal. This bit is default 0.

Bit 0: AUXFANIN1 Input Control. Set to 1, pin58 (AUXFANIN1) acts as FAN tachometer input, which is default value. Set to 0, this pin58 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

Note : Please refer to Bank0 Index 5Dh , Fan divisor table.

6.8.40 Serial Bus Address Register - Index 48h (Bank 0)

Register Location: 48h
Power on Default Value: 2Dh
Attribute: Read/Write
Size: 8 bits



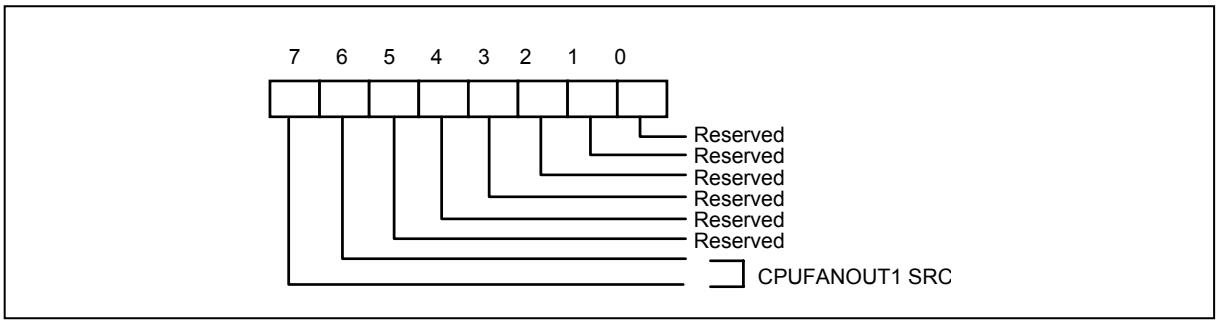
Bit 7: Reserved (Read Only).

Bit 6-0: Serial Bus address <7:1>.

6.8.41 Reserved - Index 49h (Bank 0)

6.8.42 CPUFANOUT1 with Temperature source Select - Index 4Ah (Bank 0)

Register Location: 4Ah
Power on Default Value: 64h
Attribute: Read/Write
Size: 8 bits



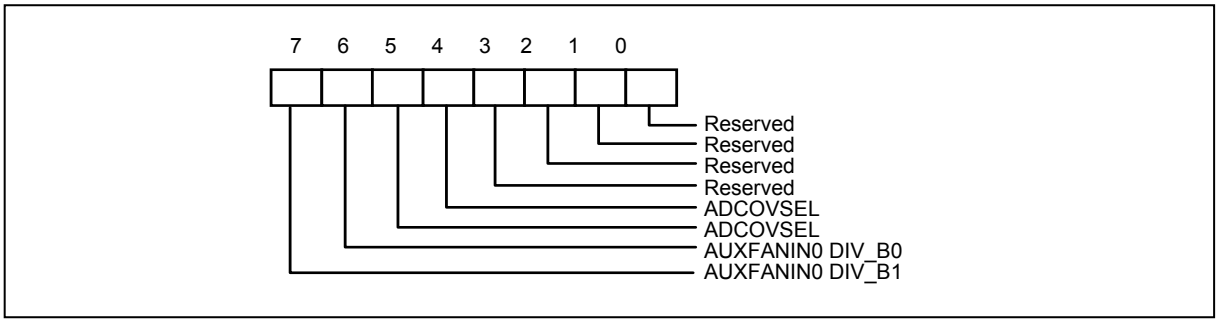
Bit 7-2: Reserved.

Bit 1-0: Select Temperature source for CPUFANOUT1 at Thermal Cruise mode or SMART FAN™ III Mode

<1:0> = 00 – SYSTIN.
<1:0> = 01 - CPUTIN.(Default)
<1:0> = 10 - AUXTIN.
<1:0> = 11 – Reserved.

6.8.43 Fan Divisor Register II - Index 4Bh (Bank 0)

Register Location: 4Bh
Power on Default Value: 44h
Attribute: Read/Write
Size: 8 bits



Bit 7-6: AUXFANIN0 Divisor bit1:0.

Note : Please refer to Bank0 Index 5Dh , Fan divisor table.

Bit 5-4: Select A/D Converter Clock Input.

<5:4> = 00 - default. ADC clock select 22.5 Khz.

<5:4> = 01- ADC clock select 5.6 Khz. (22.5K/4)

<5:4> = 10 - ADC clock select 1.4Khz. (22.5K/16)

<5:4> = 11 - ADC clock select 0.35 Khz. (22.5K/64)

Bit 3-2: These two bits should be set to 01h. The default value is 01h.

Bit 1-0: Reserved.

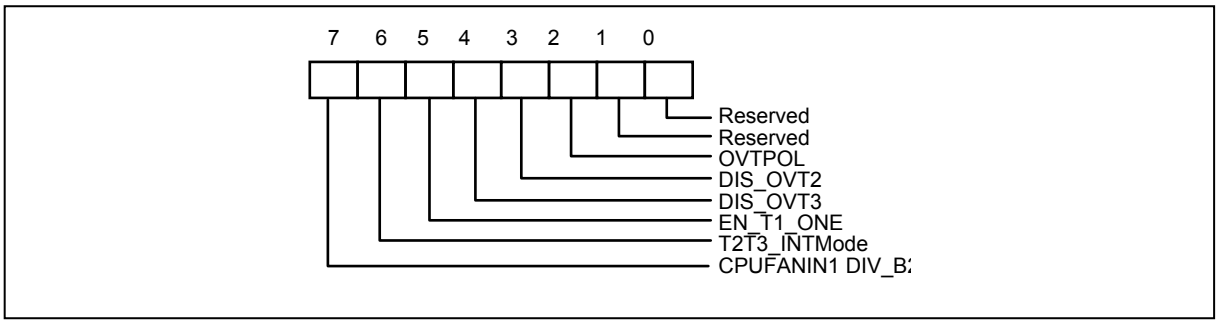
6.8.44 SMI#/OVT# Control Register - Index 4Ch (Bank 0)

Register Location: 4Ch

Power on Default Value: 10h

Attribute: Read/Write

Size: 8 bits



Bit 7: CPUFANIN1 Divisor bit2.

Bit 6: Set to 1, the SMI# output type of Temperature CPUTIN/AUXTIN is set to Comparator Interrupt mode. Set to 0, the SMI# output type is set to Two-Times Interrupt mode. (default 0)

Bit 5: Set to 1, the SMI# output type of temperature SYSTIN is One-Time interrupt mode. Set to 0, the SMI# output type is Two-Times interrupt mode.

Bit 4: Disable temperature sensor AUXTIN over-temperature (OVT) output if set to 1. Set to 0, enable AUXTIN OVT output through pin OVT#. (default 1)

Bit 3: Disable temperature sensor CPUTIN over-temperature (OVT) output if set to 1. Set to 0, enable CPUTIN OVT output through pin OVT#. (default 0)

Bit 2: Over-temperature polarity. Write 1, OVT# active high. Write 0, OVT# active low. (default 0)

Bit 1-0: Reserved.

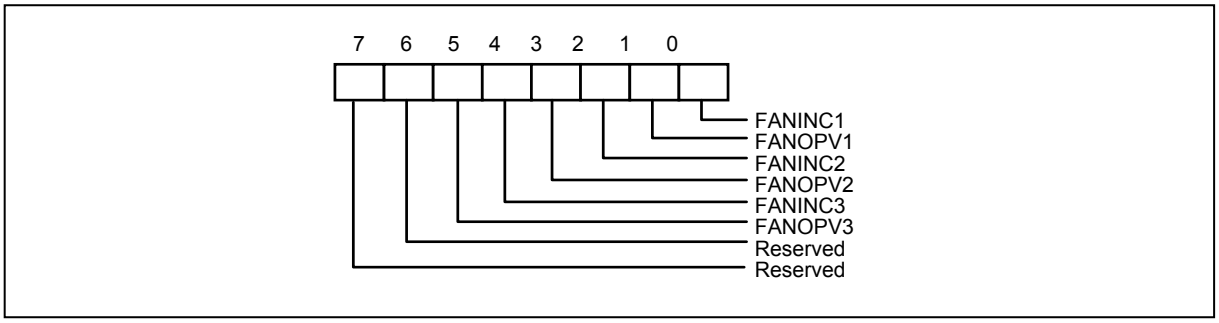
6.8.45 FAN IN/OUT Control Register - Index 4Dh (Bank 0)

Register Location: 4Dh

Power on Default Value: 15h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: Reserved.

Bit 5: AUXFANIN0 output value if bit 4 sets to 0. Write 1, pin111(AUXFANIN0) always generates a logic high signal. Write 0, pin111 always generates a logic low signal. This bit is default 0.

Bit 4: AUXFANIN0 Input Control. Set to 1, pin111(AUXFANIN) acts as FAN tachometer input, which is default value. Set to 0, this pin111 acts as FAN control signal and the output value of FAN control is set by this register bit 5.

Bit 3: CPUFANIN0 output value if bit 2 sets to 0. Write 1, pin112(CPUFANIN0) always generates a logic high signal. Write 0, pin112 always generates a logic low signal. This bit is default 0.

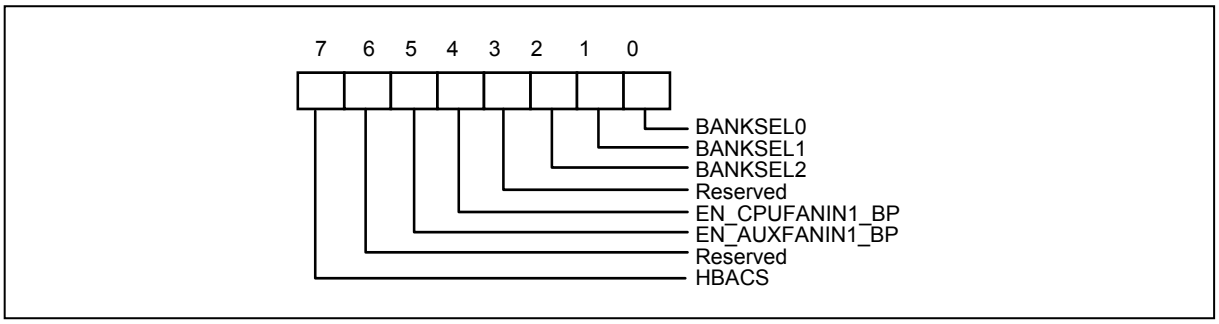
Bit 2: CPUFANIN0 Input Control. Set to 1, pin112(CPUFANIN0) acts as FAN tachometer input, which is default value. Set to 0, this pin112 acts as FAN control signal and the output value of FAN control is set by this register bit 3.

Bit 1: SYSFANIN output value if bit 0 sets to 0. Write 1, pin113(SYSFANIN) always generates a logic high signal. Write 0, pin113 always generates a logic low signal. This bit is default 0.

Bit 0: SYSFANIN Input Control. Set to 1, pin113(SYSFANIN) acts as FAN tachometer input, which is default value. Set to 0, this pin113 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

6.8.46 Register 50h ~ 5Fh Bank Select Register - Index 4Eh (Bank 0)

Register Location: 4Eh
Power on Default Value: 80h
Attribute: Read/Write
Size: 8 bits



Bit 7: HBACS - High byte access. Set to 1, access Index 4Fh high byte register. Set to 0, access Index 4Fh low byte register. (default 1)

Bit 6: Reserved. This bit should be set to 0.

Bit 5: BEEP output control for AUXFANIN1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for CPUFANIN1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: Reserved. This bit should be set to 0.

Bit 2-0: Index ports 0x50~0x5F Bank select.

Set to 0, select Bank0.

Set to 1, select Bank1.

Set to 2, select Bank2.

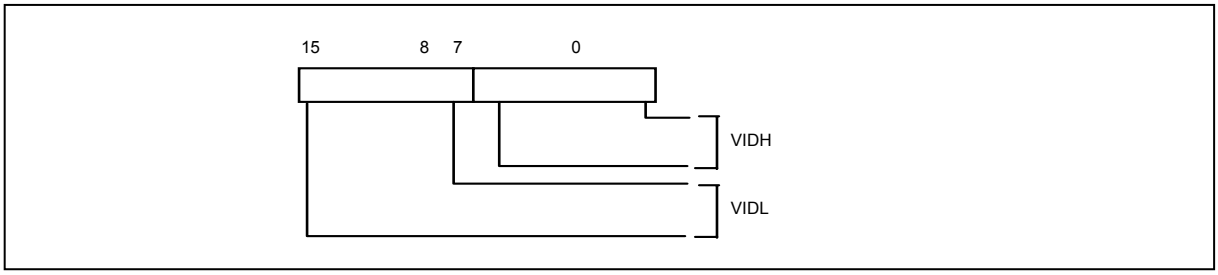
6.8.47 Winbond Vendor ID Register - Index 4Fh (Bank 0)

Register Location: 4Fh

Power on Default Value: <15:0> = 5CA3h

Attribute: Read Only

Size: 16 bits



Bit 15-8: Vendor ID High Byte if Index 4Eh.bit7=1. Default 5Ch.

Bit 7-0: Vendor ID Low Byte if Index 4Eh.bit7=0. Default A3h.

6.8.48 Winbond Test Register - Index 50h-55h (Bank 0)

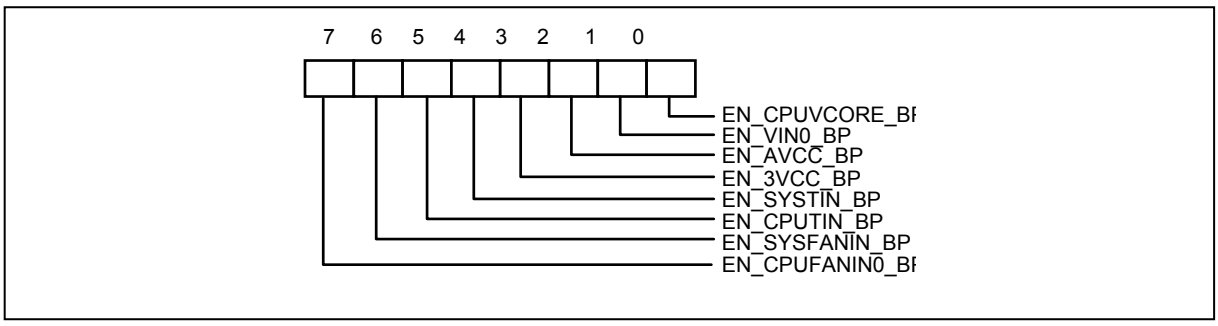
6.8.49 BEEP Control Register 1 - Index 56h (Bank 0)

Register Location: 56h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: BEEP output control for CPUFANIN0 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 6: BEEP output control for SYSFANIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 5: BEEP output control for temperature CPUTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for temperature SYSTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for 3VCC if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

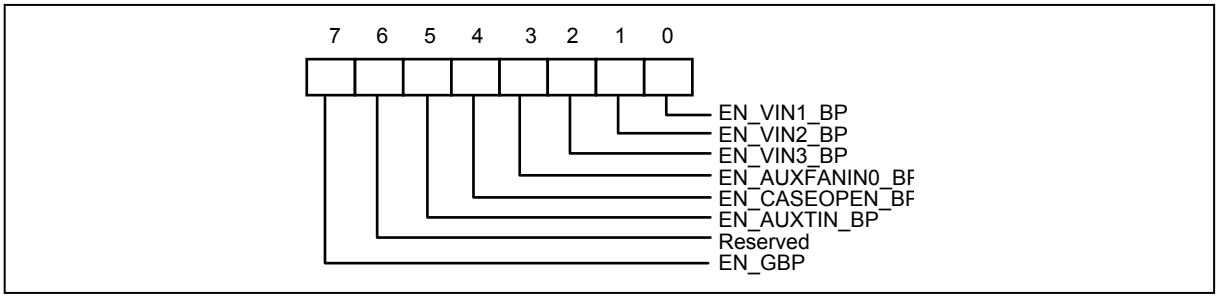
Bit 2: BEEP output control for AVCC if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 1: BEEP output control for VIN0 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for CPUVCORE if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

6.8.50 BEEP Control Register 2 - Index 57h (Bank 0)

Register Location: 57h
Power on Default Value: 80h
Attribute: Read/Write
Size: 8 bits



Bit 7: Global BEEP Control. Write 1, enable global BEEP output, which is default value. Write 0, disable all BEEP output.

Bit 6: Reserved.

Bit 5: BEEP output control for temperature AUXTIN if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for CASEOPEN if case has been opened. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for AUXFANIN0 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

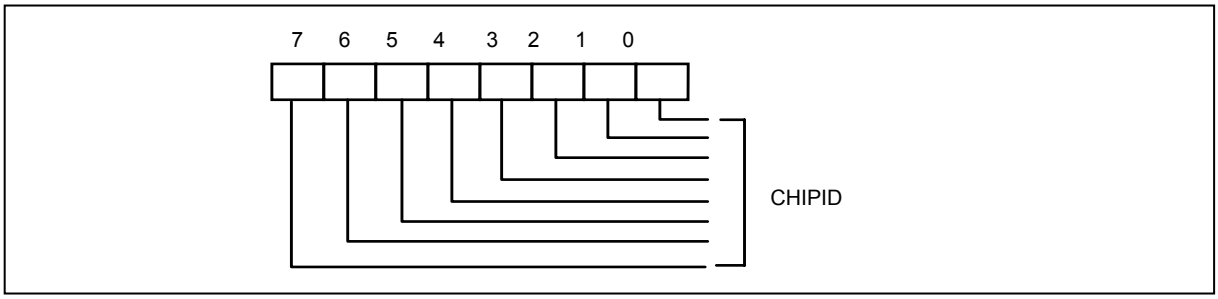
Bit 2: BEEP output control for VIN3 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 1: BEEP output control for VIN2 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for VIN1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

6.8.51 Chip ID - Index 58h (Bank 0)

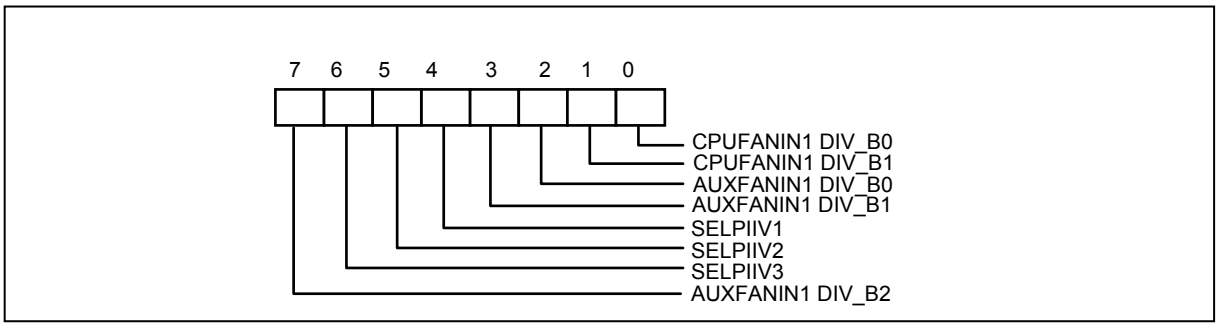
Register Location: 58h
Power on Default Value: A1h
Attribute: Read Only
Size: 8 bits



Bit 7-0: Winbond Chip ID number. Read this register will return A1h.

6.8.52 Diode Selection Register - Index 59h (Bank 0)

Register Location: 59h
Power on Default Value: 70h
Attribute: Read/Write
Size: 8 bits



Bit 7: AUXFANIN1 Divisor bit2.

Bit 6: Diode mode selection of temperature AUXTIN if Index 5Dh bit3 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode.

Bit 5: Diode mode selection of temperature CPUTIN if Index 5Dh bit2 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode.

Bit 4: Diode mode selection of temperature SYSTIN if Index 5Dh bit1 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode.

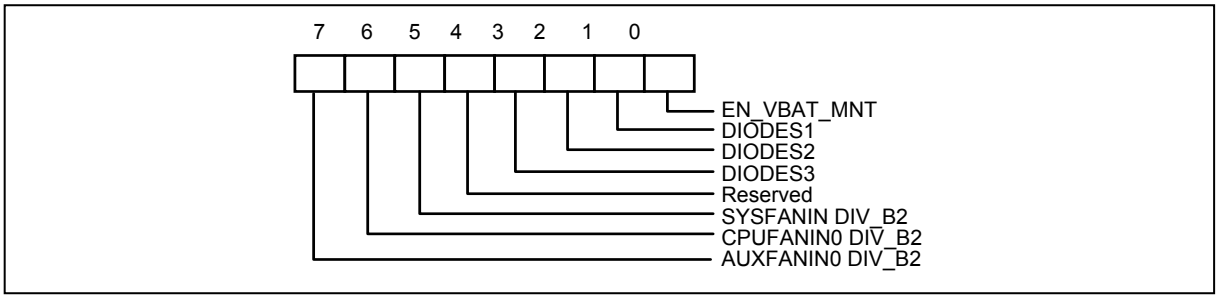
Bit 3-2: AUXFANIN1 Divisor bit 1:0.

Bit 1-0: CPUFANIN1 Divisor bit 1:0.

6.8.53 Reserved - Index 5Ah-5Ch (Bank 0)

6.8.54 VBAT Monitor Control Register - Index 5Dh (Bank 0)

Register Location: 5Dh
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: AUXFANIN0 Divisor bit2.

Bit 6: CPUFANIN0 Divisor bit2.

Bit 5: SYSFANIN Divisor bit2.

Bit 4: Reserved.

Bit 3: Sensor type selection of AUXTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 2: Sensor type selection of CPUTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 1: Sensor type selection of SYSTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 0: Set to 1, enable battery voltage monitor. Set to 0, disable battery voltage monitor. After set this bit from 0 to 1, the monitored value will be updated to the VBAT reading value register after one monitor cycle time.

Fan divisor table :

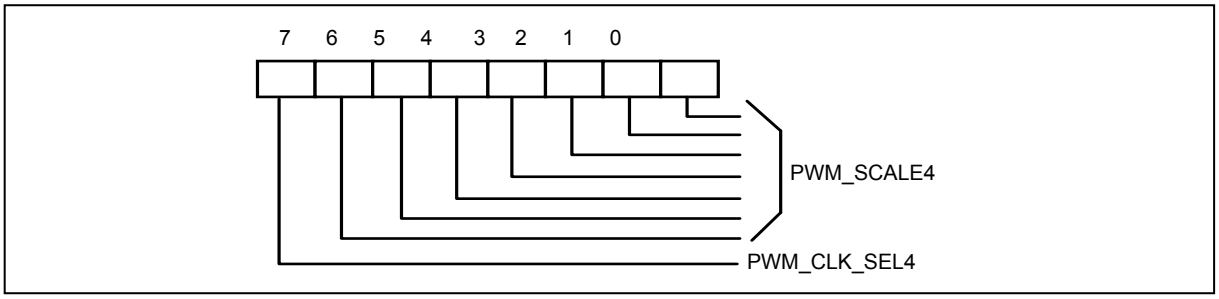
BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	***1***	1	0	0	***16***
0	0	1	***2***	1	0	1	***32***
0	1	0	***4***	1	1	0	***64***
0	1	1	***8***	1	1	1	***128***

Table 6.3

6.8.55 Reserved Register - Index 5Eh-5Fh (Bank 0)

6.8.56 CPUFANOUT1 PWM Output Frequency Configuration Register - Index 60h (Bank 0)

Register Location: 60h
Power on Default Value: 04h
Attribute: Read/Write
Size: 8 bits



The register is meaningful when CPUFANOUT1 be programmed as PWM output.

Bit 7: CPUFANOUT1 PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

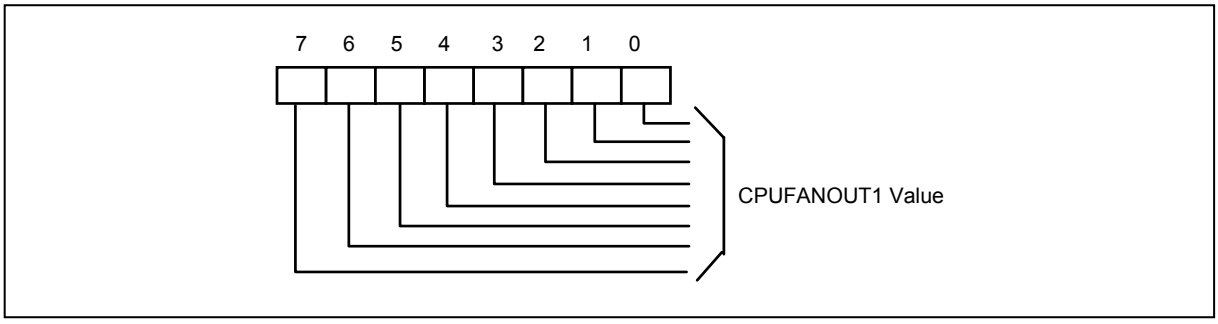
Bit 6-0: CPUFANOUT1 PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1
02h : divider is 2
03h : divider is 3
:
:

the formula is $$\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$$

6.8.57 CPUFANOUT1 Output Value Select Register - Index 61h (Bank 0)

Register Location: 61h
Power on Default Value: FFh
Attribute: Read/Write
Size: 8 bits



(1)If CPUFANOUT1 be programmed as PWM output (Bank0 Index 62h.bit6 is 0)

Bit 7-0: CPUFANOUT1 PWM Duty Cycle. Write FFh, CPUFANOUT1 duty cycle is 100%. Write 00h, CPUFANOUT1 duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If CPUFANOUT1 be programmed as DC Voltage output (Bank0 Index 62h.bit6 is 1)

Bit 7-2: CPUFANOUT1 voltage control.

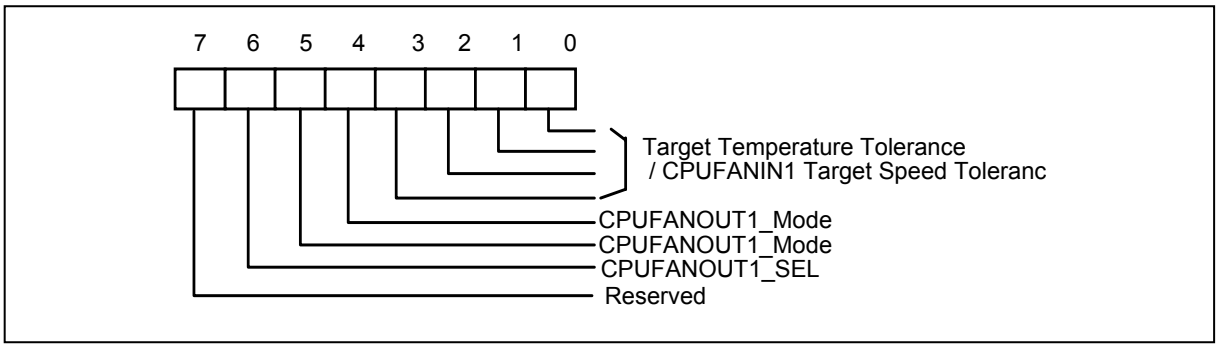
Bit 1-0: Reserved.

$$\textbf{OUTPUT Voltage} = AVCC * \frac{FANOUT}{64}$$

Note. See the Table 6.4

6.8.58 FAN Configuration Register III - Index 62h (Bank 0)

Register Location:	62h
Power on Default Value:	40h
Attribute:	Read/Write
Size:	8 bits



Bit7 : Reserved.

Bit 6: CPUFANOUT1 output mode selection. Set to 0, CPUFANOUT1 pin is as PWM output duty cycle so that it can drive a logical high or low signal. Set to 1, CPUFANOUT1 pin is as DC voltage output which can provide analog voltage output. (Default 1)

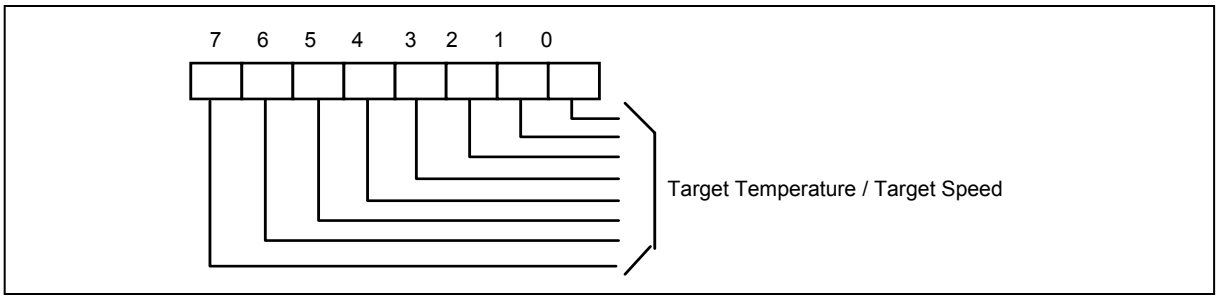
Bit 5-4: CPUFANOUT1 mode control.

Set 00, CPUFANOUT1 is as Manual Mode. (Default).
Set 01, CPUFANOUT1 is as Thermal Cruise Mode.
Set 10, CPUFANOUT1 is as Fan Speed Cruise Mode.
Set 11, CPUFANOUT1 is SMART FAN™ III Mode.

(1)When at Thermal Cruise mode or SMART FAN™ III mode:
Bit3-0: Tolerance of select temperature source Target Temperature.
(2)When at Fan Speed Cruise mode:
Bit3-0: Tolerance of CPUFANIN1 Target Speed.

6.8.59 Target Temperature Register/ CPUFANIN1 Target Speed Register - Index 63h (Bank 0)

Register Location: 63h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits

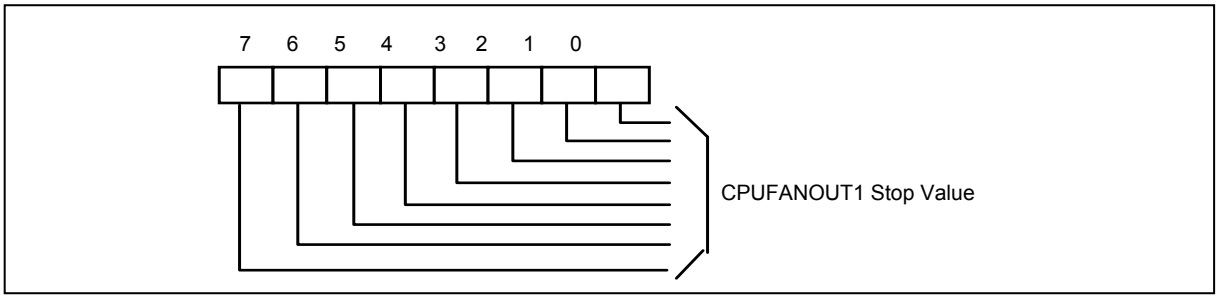


(1)When at Thermal Cruise mode or SMART FAN™ III mode:
Bit 7: Reserved.
Bit 6-0: Target Temperature of select temperature source.

(2)When at Fan Speed Cruise mode:
Bit 7-0: CPUFANIN1 Target Speed.

6.8.60 CPUFANOUT1 Stop Value Register - Index 64h (Bank 0)

Register Location: 64h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits

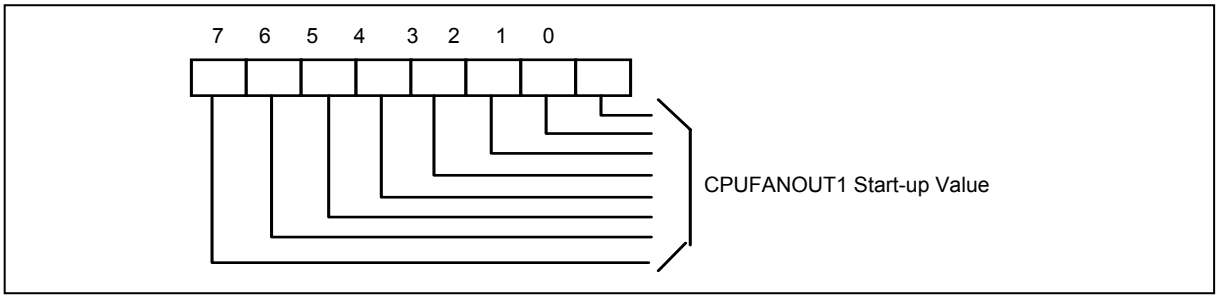


When at Thermal Cruise mode or SMART FAN™ III mode, CPUFANOUT1 value will decrease to this value. This register should be written a non-zero minimum stop value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

6.8.61 CPUFANOUT1 Start-up Value Register - Index 65h (Bank 0)

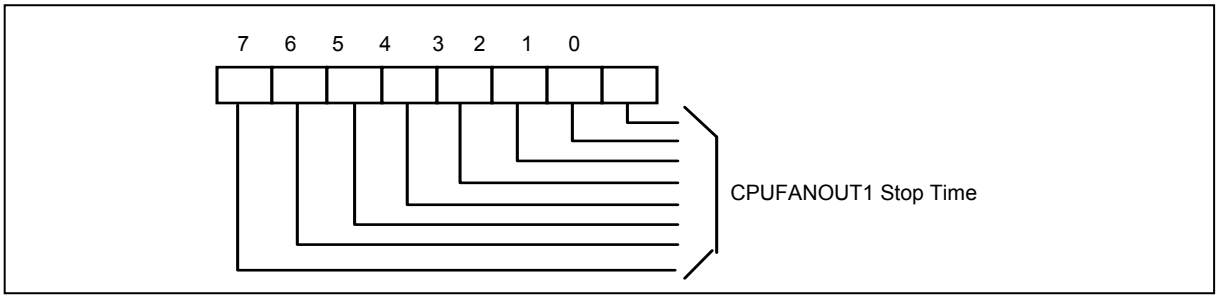
Register Location: 65h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode, CPUFANOUT1 value will increase from 0 to this register value to provide a minimum value to turn on the fan.

6.8.62 CPUFANOUT1 Stop Time Register - Index 66h (Bank 0)

Register Location: 66h
Power on Default Value: 3Ch
Attribute: Read/Write
Size: 8 bits



When at Thermal Cruise mode or SMART FAN™ III mode, this register determines the time of which CPUFANOUT1 value is from stop value to 0.

(1)When at PWM output:

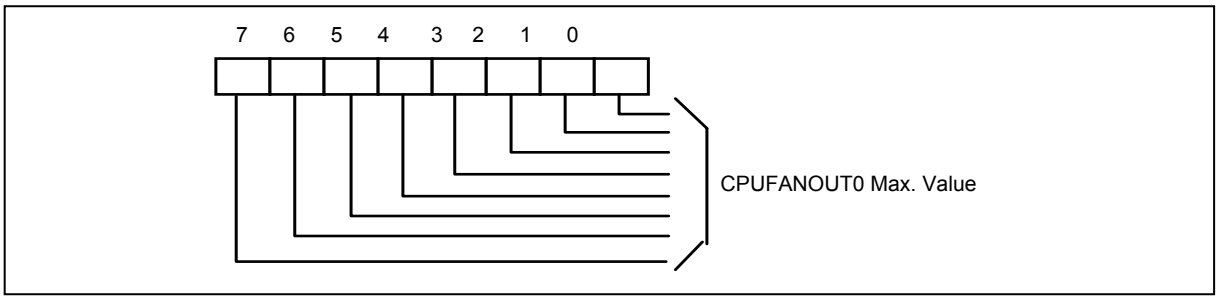
The unit of this register is 0.1 second. The default time is 6 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 24 seconds.

6.8.63 CPUFANOUT0 Maximum Output Value Register - Index 67h (Bank 0)

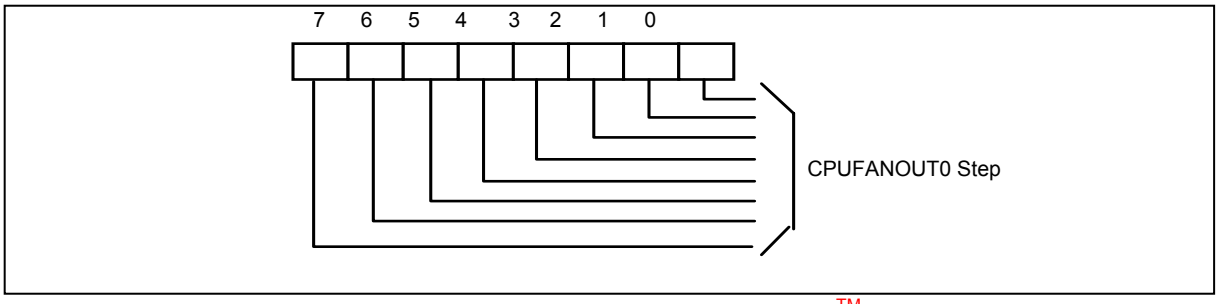
Register Location: 67h
Power on Default Value: FFh
Attribute: Read/Write
Size: 8 bits



When at SMART FAN™ III mode, CPUFANOUT0 value will increase to this value. This register should be written a non-zero value that cannot lower than Stop value.

6.8.64 CPUFANOUT0 Output Step Value Register - Index 68h (Bank 0)

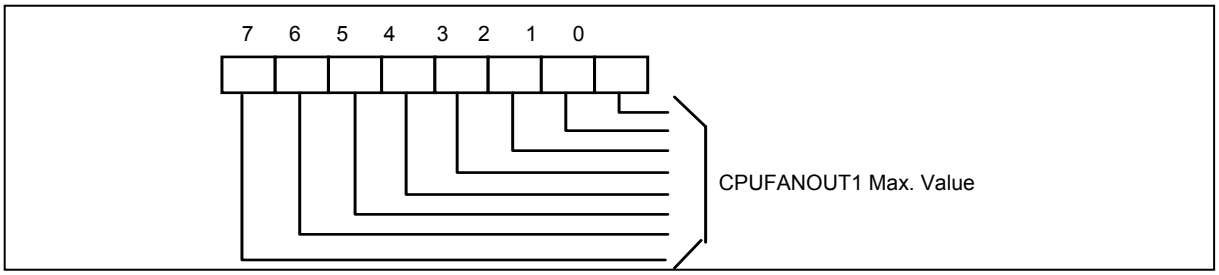
Register Location: 68h
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits



This register determines the value that CPUFANOUT0 in SMART FAN™ III mode decreased or increased to the next speed.

6.8.65 CPUFANOUT1 Maximum Output Value Register - Index 69h (Bank 0)

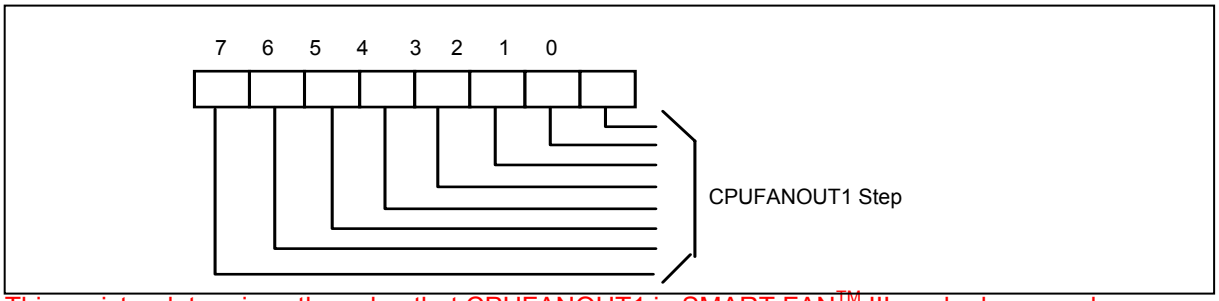
Register Location: 69h
Power on Default Value: FFh
Attribute: Read/Write
Size: 8 bits



When at SMART FAN™ III mode, CPUFANOUT1 value will increase to this value. This register should be written a non-zero value that cannot lower than Stop value.

6.8.66 CPUFANOUT1 Output Step Value Register - Index 6Ah (Bank 0)

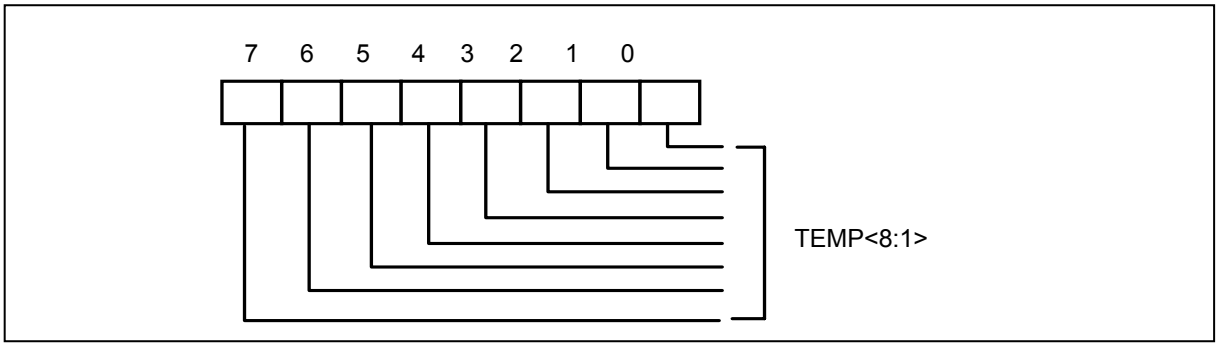
Register Location: 6Ah
Power on Default Value: 01h
Attribute: Read/Write
Size: 8 bits



This register determines the value that CPUFANOUT1 in SMART FAN™ III mode decreased or increased to the next speed.

6.8.67 CPUTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (Bank 1)

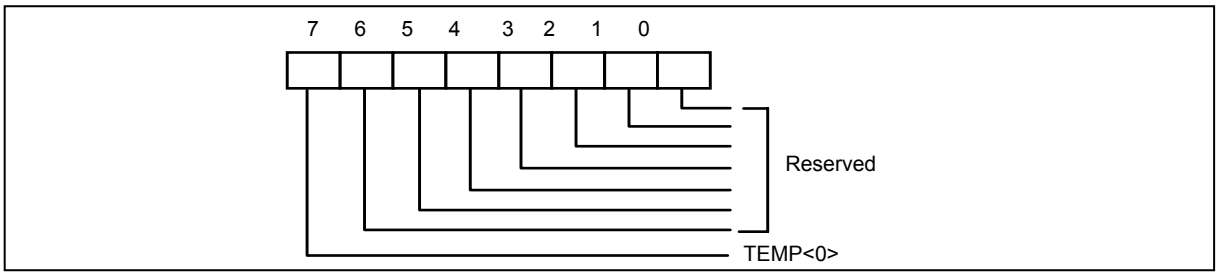
Register Location: 50h
Attribute: Read Only
Size: 8 bits



Bit 7-0: Temperature <8:1> of CPUTIN sensor, which is high byte, means 1°C.

6.8.68 CPUTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (Bank 1)

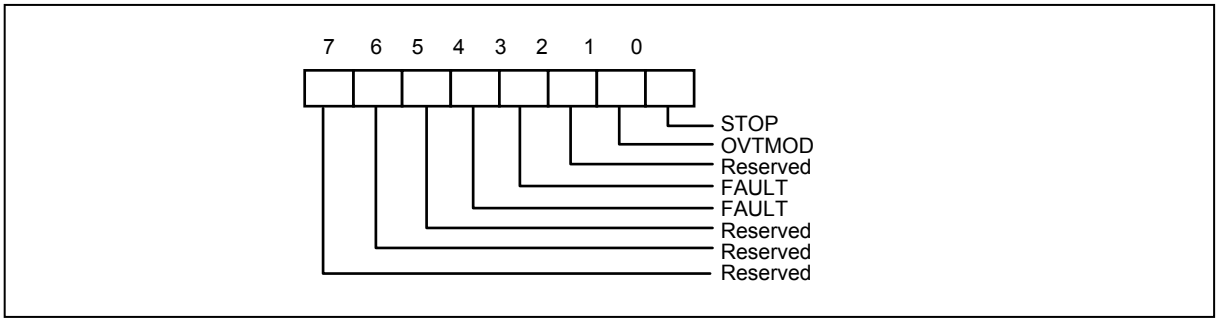
Register Location: 51h
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <0> of CPUTIN sensor, which is low byte, means 0.5°C.
Bit 6-0: Reserved.

6.8.69 CPUTIN Temperature Sensor Configuration Register - Index 52h (Bank 1)

Register Location: 52h
Power on Default Value: 00h
Size: 8 bits



Bit 7-5: Read Only - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

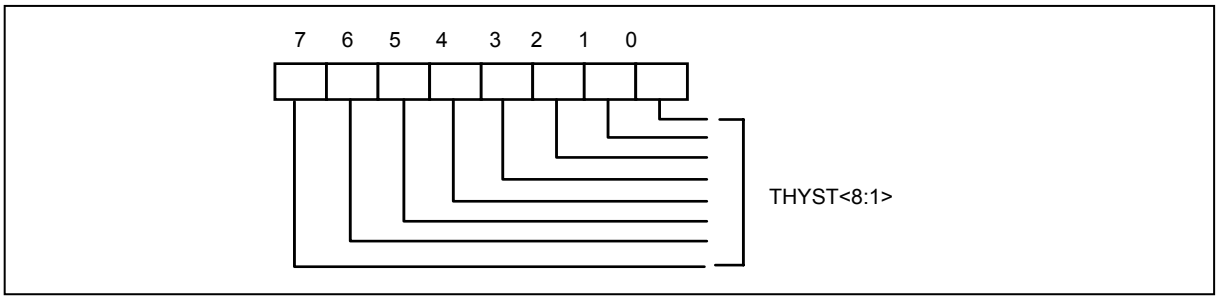
Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

6.8.70 CPUTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (Bank 1)

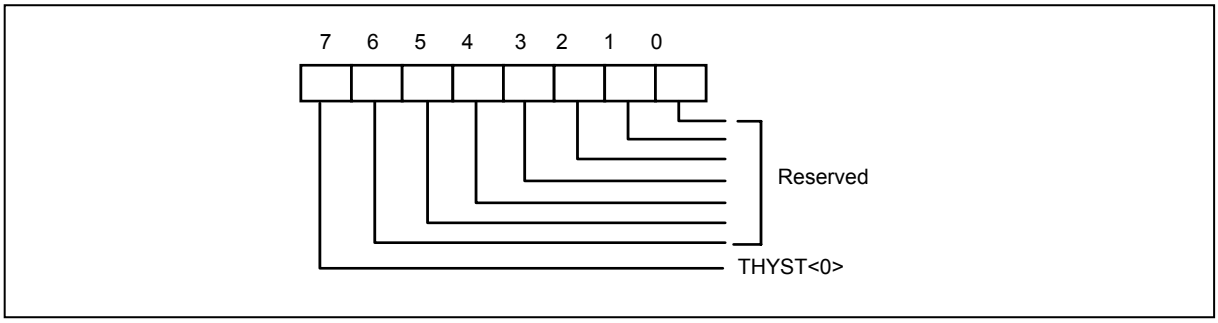
Register Location: 53h
Power on Default Value: 4Bh
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

6.8.71 CPUTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (Bank 1)

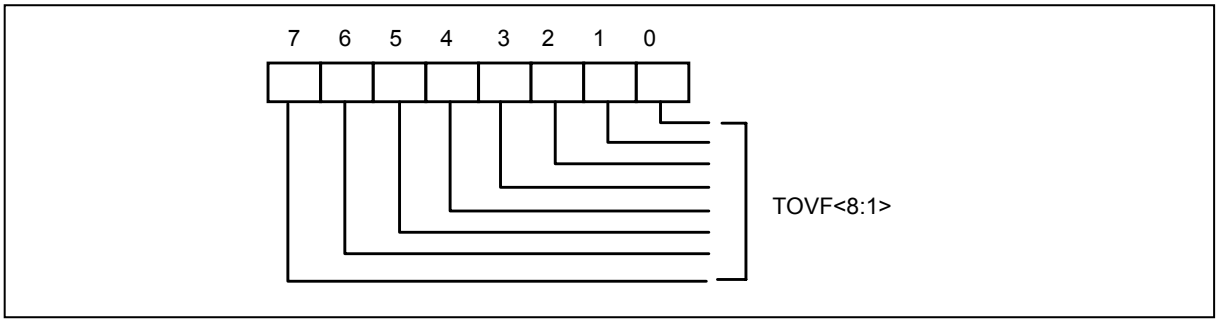
Register Location: 54h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Hysteresis temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

6.8.72 CPUTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (Bank1)

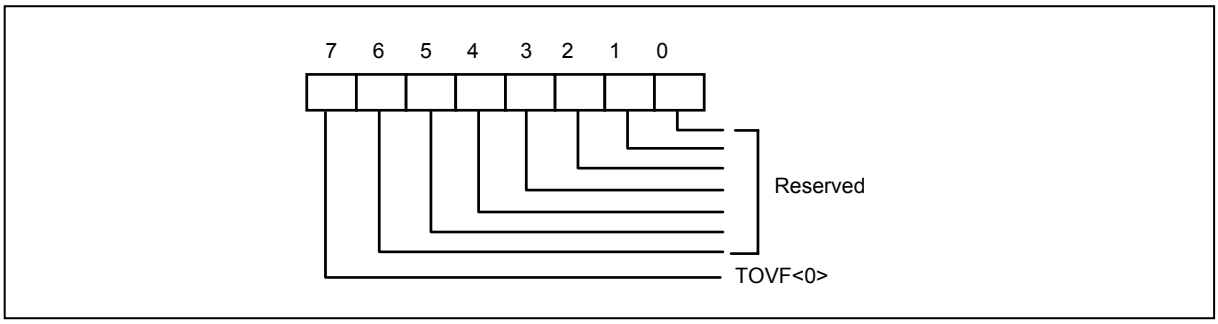
Register Location: 55h
Power on Default Value: 50h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

6.8.73 CPUTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (Bank 1)

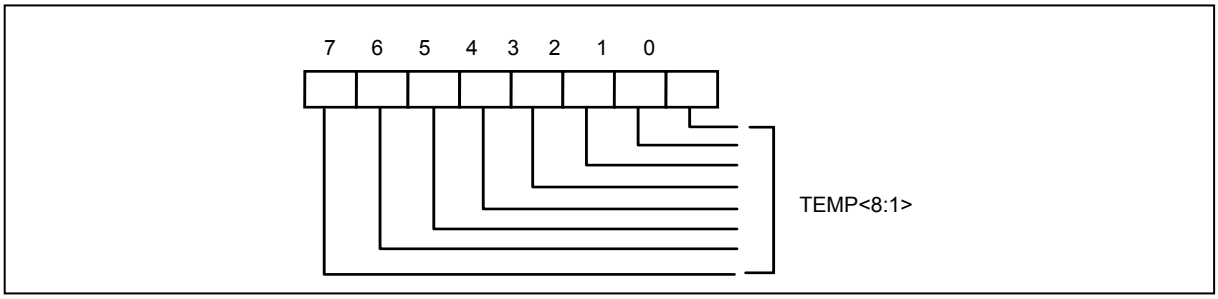
Register Location: 56h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Over-temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

6.8.74 AUXTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (Bank 2)

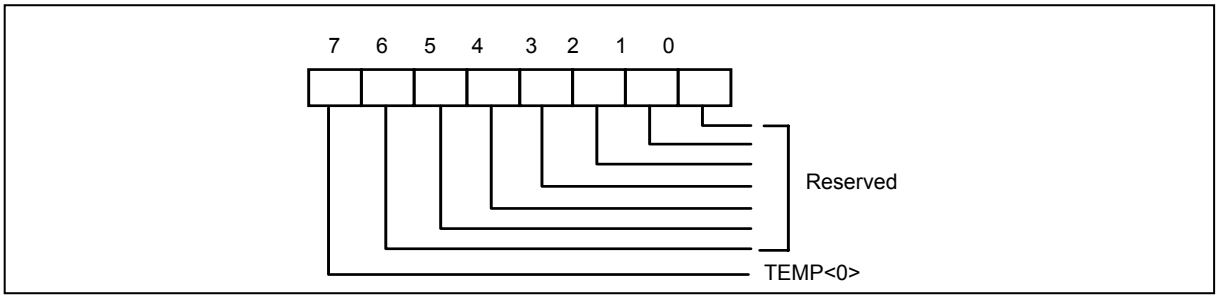
Register Location: 50h
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <8:1> of AUXTIN sensor, which is high byte, means 1°C.

6.8.75 AUXTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (Bank 2)

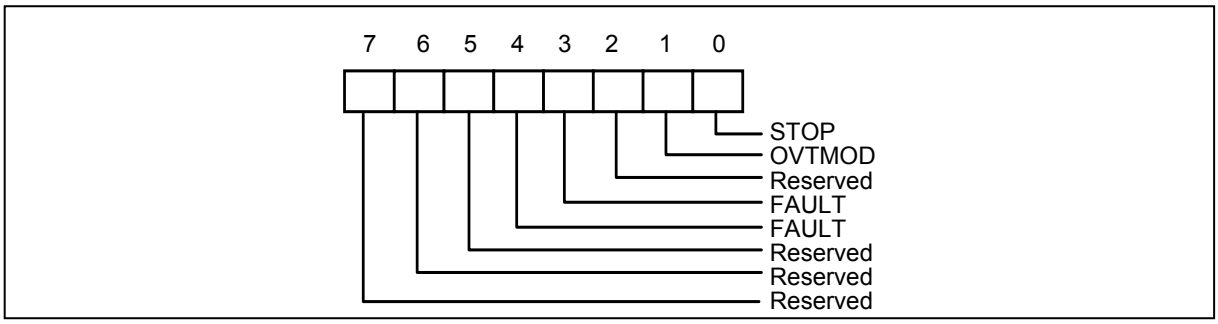
Register Location: 51h
Attribute: Read Only
Size: 8 bits



Bit 7: Temperature <0> of AUXTIN sensor, which is low byte, means 0.5°C.
Bit 6-0: Reserved.

6.8.76 AUXTIN Temperature Sensor Configuration Register - Index 52h (Bank 2)

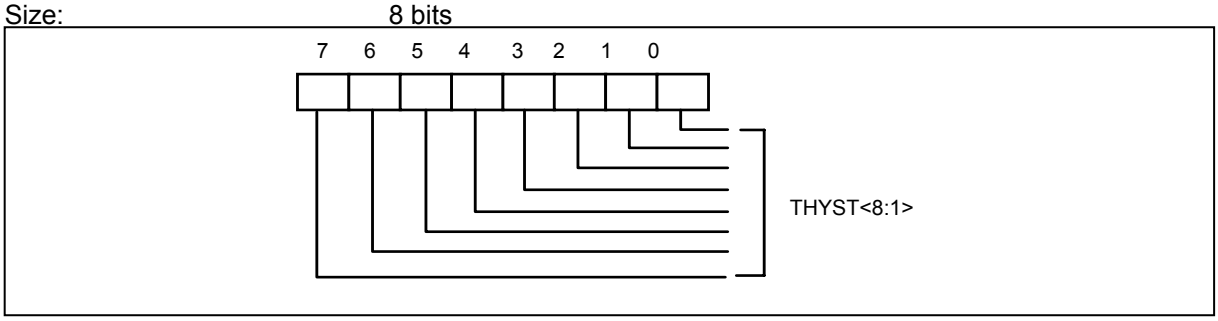
Register Location: 52h
Power on Default Value: 00h
Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.
Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.
Bit 2: Read - Reserved. This bit should be set to 0.
Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.
Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

6.8.77 AUXTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (Bank 2)

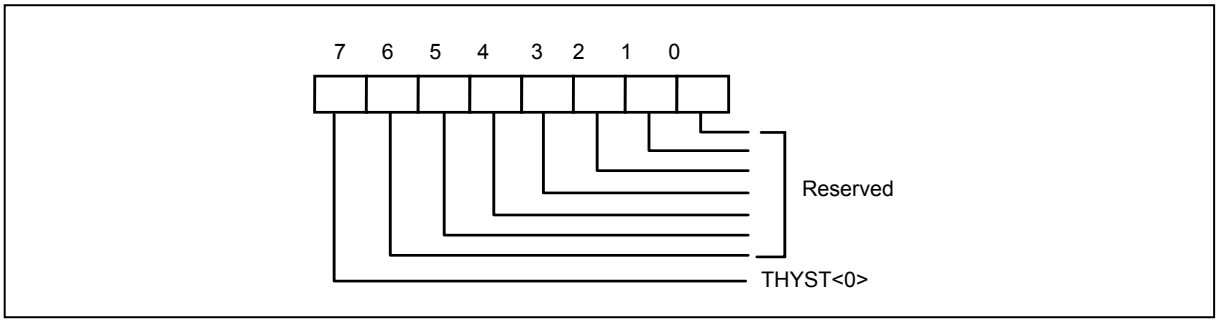
Register Location: 53h
Power on Default Value 4Bh
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

6.8.78 AUXTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (Bank 2)

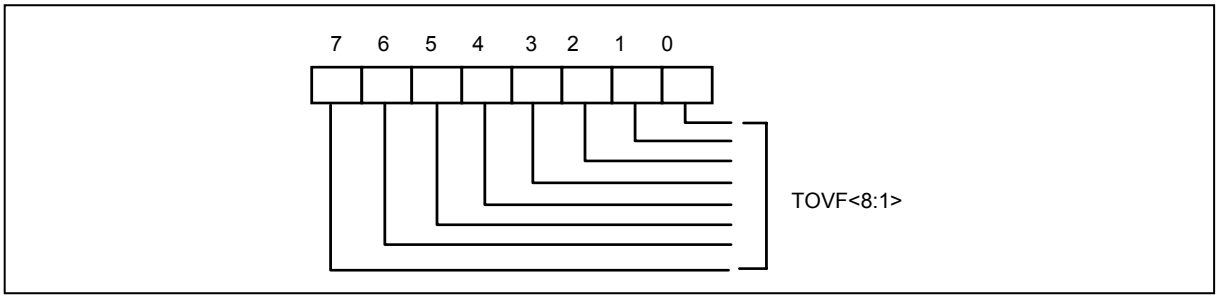
Register Location: 54h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Hysteresis temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

6.8.79 AUXTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (Bank 2)

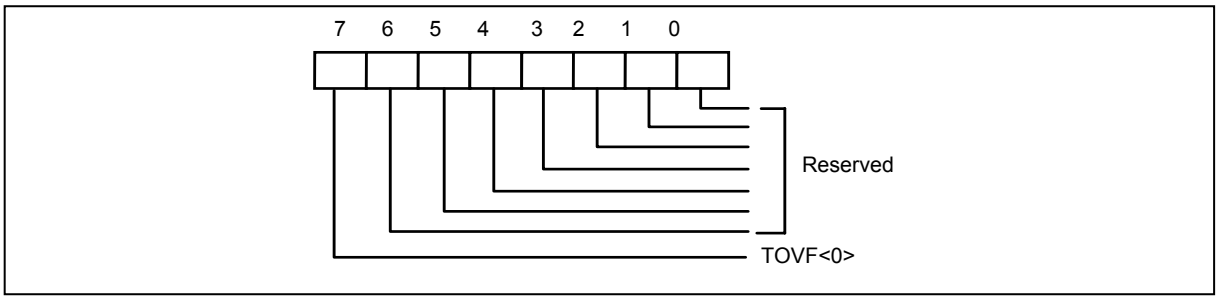
Register Location: 55h
Power on Default Value: 50h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

6.8.80 AUXTIN Temperature Sensor Over-temperature(Low Byte) Register - Index 56h (Bank 2)

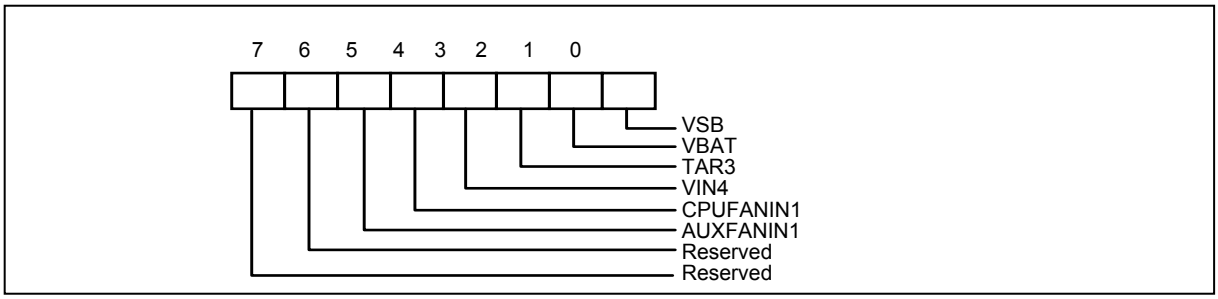
Register Location: 56h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7: Over-temperature bit 0, which is low Byte.
Bit 6-0: Reserved.

6.8.81 Interrupt Status Register 3 - Index 50h (Bank 4)

Register Location: 50h
Power on Default Value: 00h
Attribute: Read Only
Size: 8 bits



Bit 7-6: Reserved.

Bit 5: A one indicates the fan count limit of AUXFANIN1 has been exceeded .

Bit 4: A one indicates the fan count limit of CPUFANIN1 has been exceeded .

Bit 3: A one indicates a High or Low limit of VIN4 has been exceeded.

Bit 2: A one indicates that the AUXTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 1: A one indicates a High or Low limit of VBAT has been exceeded.

Bit 0: A one indicates a High or Low limit of VSB has been exceeded.

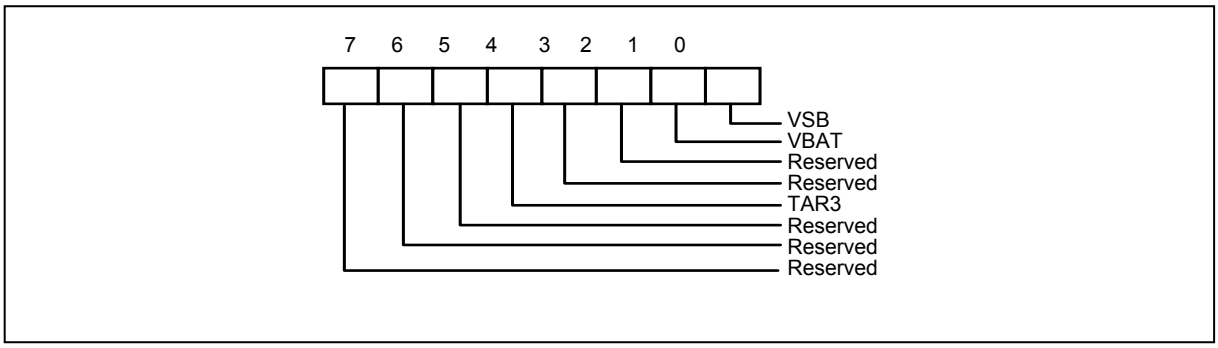
6.8.82 SMI# Mask Register 4 - Index 51h (Bank 4)

Register Location: 51h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-5: Reserved.

Bit 4: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 3-2: Reserved.

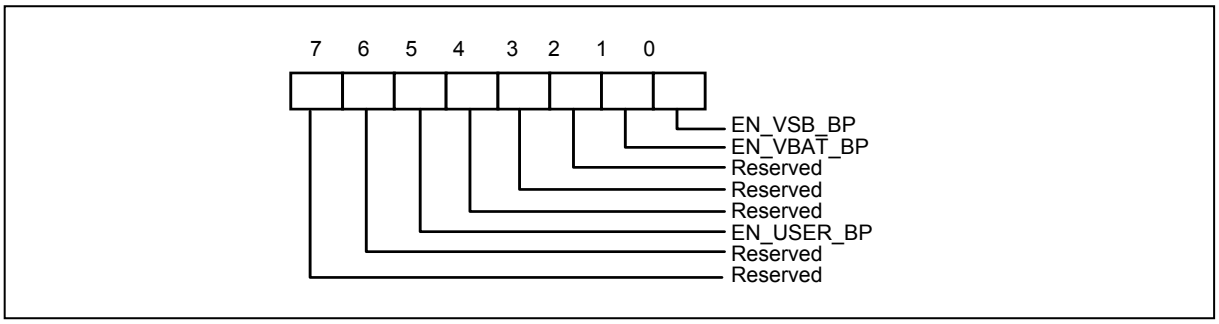
Bit 1: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

6.8.83 Reserved Register - Index 52h (Bank 4)

6.8.84 BEEP Control Register 3 - Index 53h (Bank 4)

Register Location: 53h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7-6: Reserved.

Bit 5: User define BEEP output function. Write 1, the BEEP is always active. Write 0, this function is inactive. (Default 0)

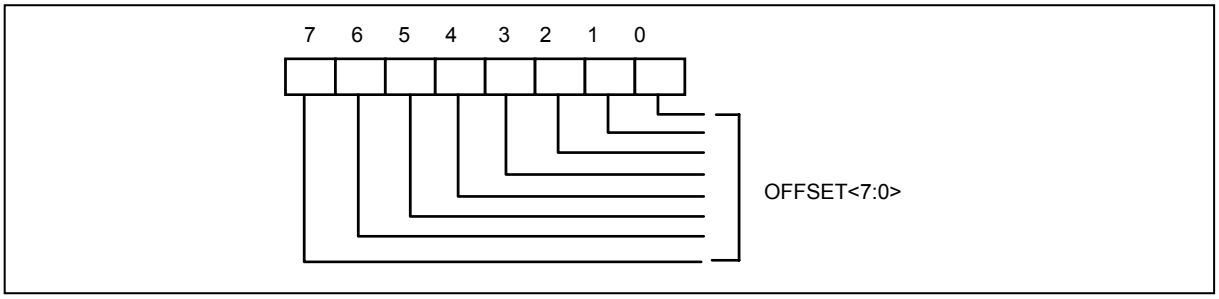
Bit 4-2: Reserved.

Bit 1: BEEP output control for VBAT if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for VSB if the monitor value exceed the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

6.8.85 SYSTIN Temperature Sensor Offset Register - Index 54h (Bank 4)

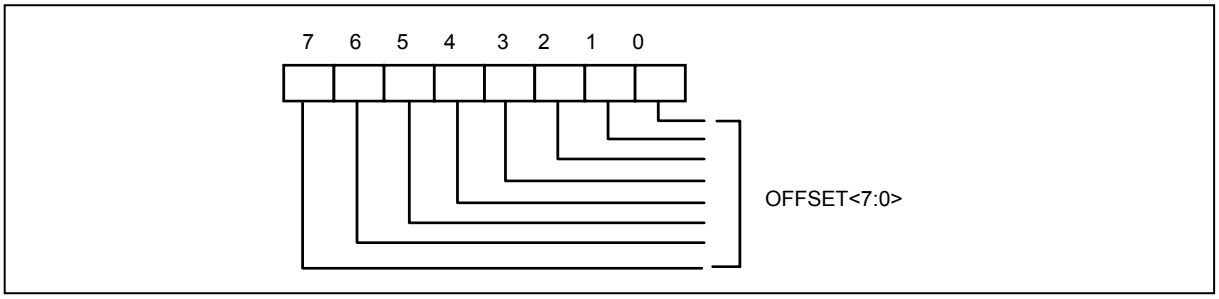
Register Location: 54h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: SYSTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

6.8.86 CPUTIN Temperature Sensor Offset Register - Index 55h (Bank 4)

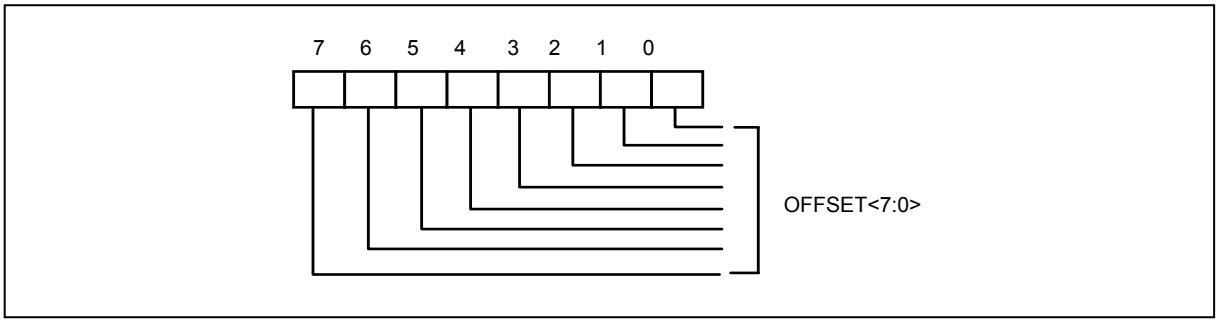
Register Location: 55h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits



Bit 7-0: CPUTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

6.8.87 AUXTIN Temperature Sensor Offset Register - Index 56h (Bank 4)

Register Location: 56h
Power on Default Value: 00h
Attribute: Read/Write
Size: 8 bits

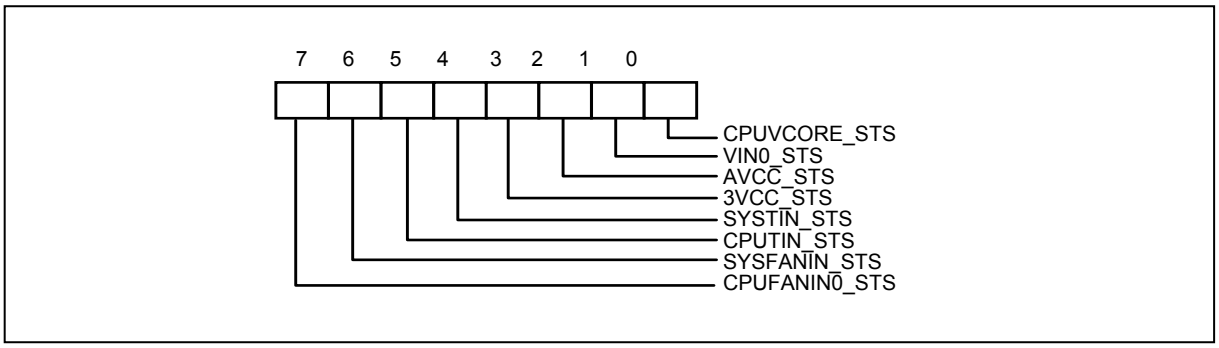


Bit 7-0: AUXTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

6.8.88 Reserved Register - Index 57h-58h (Bank 4)

6.8.89 Real Time Hardware Status Register I - Index 59h (Bank 4)

Register Location: 59h
Power on Default Value: 00h
Attribute: Read Only
Size: 8 bits



Bit 7: CPUFANIN0 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 6: SYSFANIN status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 5: CPUTIN temperature sensor status. Read 1, the temperature exceeds the over-temperature limit value. Read 0, the temperature is in under the hysteresis value.

Bit 4: SYSTIN temperature sensor status. Read 1, the temperature exceeds the over-temperature limit value. Read 0, the temperature is in under the hysteresis value.

Bit 3: 3VCC Voltage status. Read 1, the voltage of 3VCC is over/under the limit value. Read 0, the voltage of 3VCC is in the limit range.

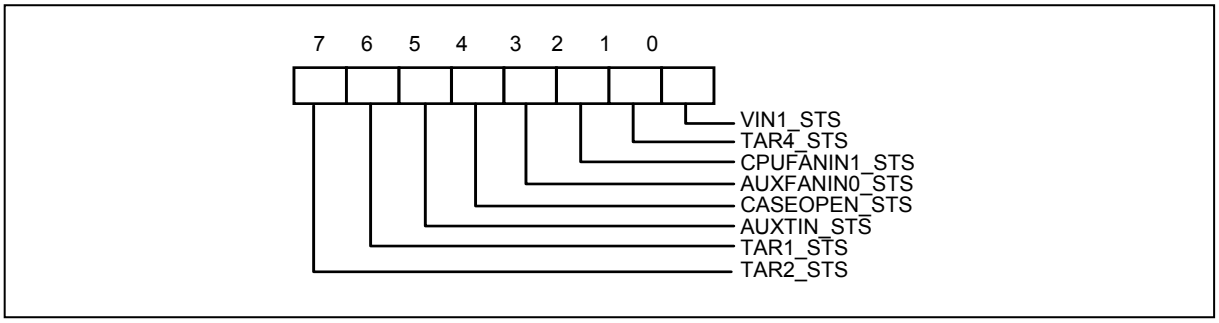
Bit 2: AVCC Voltage status. Set 1, the voltage of AVCC is over/under the limit value. Read 0, the voltage of AVCC is in the limit range.

Bit 1: VIN0 Voltage status. Set 1, the voltage of VIN0 is over/under the limit value. Read 0, the voltage of VIN0 is in the limit range.

Bit 0: CPUVCORE Voltage status. Read 1, the voltage of CPUVCORE is over/under the limit value. Read 0, the voltage of CPUVCORE is in the limit range.

6.8.90 6.8.90 Real Time Hardware Status Register II - Index 5Ah (*Bank 4*)

Register Location: 5Ah
Power on Default Value: 00h
Attribute: Read Only
Size: 8 bits



Bit 7: Smart Fan of CPUFANIN0 warning status. Read 1, the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.

Bit 6: Smart Fan of SYSFANIN warning status. Read 1, the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.

Bit 5: AUXTIN temperature sensor status. Read 1, the temperature exceeds the over-temperature limit value. Read 0, the temperature is in under the hysteresis value.

Bit 4: Case Open status. Read 1, the case open is detected and latched. Read 0, the case is not latched open.

Bit 3: AUXFANIN0 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

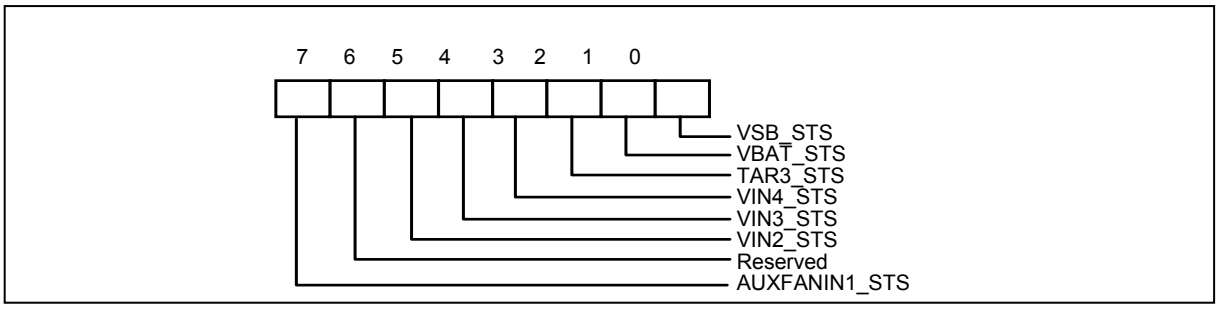
Bit 2: CPUFANIN1 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 1: Smart Fan of CPUFANIN1 warning status. Read 1, the select temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.

Bit 0: VIN1 Voltage status. Read 1, the voltage of VIN1 is over/under the limit value. Read 0, the voltage of VIN1 is in the limit range.

6.8.91 Real Time Hardware Status Register III - Index 5Bh (Bank 4)

Register Location: 5Bh
Power on Default Value: 00h
Attribute: Read Only
Size: 8 bits



Bit 7: AUXFANIN1 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 6: Reserved.
Bit 5: VIN2 Voltage status. Read 1, the voltage of VIN2 is over/under the limit value. Read 0, the voltage of VIN21 is in the limit range.
Bit 4: VIN3 Voltage status. Read 1, the voltage of VIN3 is over/under the limit value. Read 0, the voltage of VIN3 is in the limit range.
Bit 3: VIN4 Voltage status. Read 1, the voltage of VIN4 is over/under the limit value. Read 0, the voltage of VIN4 is in the limit range.
Bit 2: Smart Fan of AUXFANIN warning status. Read 1, the AUXTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.
Bit 1: VBAT Voltage status. Read 1, the voltage of VBAT is over/under the limit value. Read 0, the voltage of VBAT is in the limit range.
Bit 0: VSB Voltage status. Read 1, the voltage of VSB is over/under the limit value. Read 0, the voltage of VSB is in the limit range.

6.8.92 Reserved Register - Index 5Ch-5Dh (Bank 4)

6.8.93 Value RAM 2 — Index 50h-59h (Bank 5)

ADDRESS A6-A0	DESCRIPTION
50h	VSB reading
51h	VBAT reading. The reading is meaningless if EN_VBAT_MNT bit(Bank0 Index 5Dh.bit0) is not set.
52h	VIN4 reading
53h	AUXFANIN1 reading Note: This location stores the number of counts of the internal clock per revolution.
54h	3VSB High Limit
55h	3VSB Low Limit
56h	VBAT High Limit
57h	VBAT Low Limit
58h	VIN4 High Limit
59h	VIN4 Low Limit
5Ah	Reserved
5Bh	Reserved
5Ch	AUXFANIN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.

6.8.94 Winbond Test Register - Index 50h-57h (Bank 6)

7. Configuration Register

7.1 Chip (Global) Control Register

CR 02h. (Software Reset; Write Only)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	Write "1" Only	Software RESET.

CR 07h. (Logic Device; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Logical Device Number.

CR 20h. (Chip ID, MSB; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 88h (higher byte).

CR 21h. (Chip ID, LSB; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 6Xh (lower byte). X for IC version

CR 22h. (Device Power Down; Default FFh)

BIT	READ / WRITE	DESCRIPTION	
7	Reserved.		
6	R / W	HM Power Down.	0: Power down. 1: No power down.
5	R / W	URB Power Down.	0: Power down. 1: No power down.
4	R / W	URA Power Down.	0: Power down. 1: No power down.
3	R / W	PRT Power Down.	0: Power down. 1: No power down.
2	Reserved.		
1	Reserved.		
0	R / W	FDC Power Down.	0: Power down. 1: No power down.

CR 23h. (IPD; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	IPD (Immediate Power Down). When set to 1, whole chip is put into power down mode immediately.

CR 24h. (Global Option; Default 0100_0ss0b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	CLKSEL => Input clock rate selection = 0 The clock input on pin18 is 24MHz. = 1 The clock input on pin18 is 48MHz. (Default)
5	Reserved.	
4	R / W	Enable SYSFANOUT as Output Buffer (For H version only) =0 SYSFANOUT is Open-Drain. (Default) =1 SYSFANOUT can drive logical high or logical low.
3	R / W	Enable CPUFANOUT0 as Output Buffer (For H version only) =0 CPUFANOUT0 is Open-Drain. (Default) =1 CPUFANOUT0 can drive logical high or logical low.
2	Read Only	ENKBC => Enable keyboard controller = 0 KBC is disabled after hardware reset. = 1 KBC is enabled after hardware reset. This bit is read only, and set/reset by power-on strapping pin (PIN54; SOUTA).
1	R / W	ENROM => Enable Serial FHW = 0 ROM is disabled after hardware reset. = 1 ROM is enabled after hardware reset. This bit set/reset by power-on strapping pin (PIN52; DTRA).
0	R / W	PNPCVS => = 0 The compatible PNP address select registers have default values. = 1 The compatible PNP address select registers have no default value.

CR 25h. (Interface tri-state Enable; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	URBTRI
4	R / W	URATRI
3	R / W	PRTTRI
2~1	Reserved.	
0	R / W	FDCTRI.

CR 26h. (Global Option; Default 0s000000b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	R / W	SEL4FDD => = 0 Select two FDD mode. = 1 Select four FDD mode.
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (pin 51).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4	Reserved.	
3	R / W	DSFDLGRQ => = 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register (base address + 2) bit 3 is effective on selecting IRQ. = 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register (base address + 2) bit 3 is not effective on selecting IRQ.
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR register (base address + 2) bit 4 is effective on selecting IRQ. = 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR register (base address + 2) bit 4 is not effective on selecting IRQ.
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is effective on selecting IRQ. = 1 Disable UART A legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is not effective on selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is effective on selecting IRQ. = 1 Disable UART B legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is not effective on selecting IRQ.

CR 27h. (Reserved)

CR 28h. (Global Option; Default 50h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~5	R / W	Flash ROM size select = 00 1M = 01 2M = 10 4M (Default) = 11 8M
4	R / W	Select to enable/disable decoding of BIOS ROM range 000E xxxxh. = 0 Enable decoding of BIOS ROM range at 000E xxxxh. = 1 Disable decoding of BIOS ROM range at 000E xxxxh.
3	R / W	Select to enable/disable decoding of BIOS ROM range FFFE xxxxh. = 0 Enable decoding of BIOS ROM range at FFFE xxxxh. = 1 Disable decoding of BIOS ROM range at FFFE xxxxh.
2~0	R / W	PRTMODS2 ~ 0 => = 0xx Parallel Port Mode. = 1xx Reserved.

CR 29h. (OVT#/HM_SMI#, UART A, Game port & MIDI pin select; Default 04h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	PIN5 function select = 0 PIN5 → OVT# = 1 PIN5 → HM_SMI#.
5~4	Reserved.	
3	R / W	PIN49~54,56~57 function select = 0 PIN49~54,56~57 → UART A. = 1 PIN49~54,56~57 → GPIO6.
2~1	R / W	PIN119~120 function select
0	R / W	PIN121~128 function select = 0 PIN121~128 → Game Port. = 1 PIN121~128 → GPIO1.

Bit-2	Bit-1	PIN119~PIN120 function
0	0	PIN 119~120 → CPUFANIN1, CPUFANOUT1
0	1	PIN 119~120 → GP21, GP20
1	x	PIN 119~120 → MSI, MSO (Default)

CR 2Ah. (I^2C pin select; Default 00h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	Serial flash interface configuration register.**(VBAT)** = 0 Normal mode. = 1 Extend dummy cycle mode. ***Note: The bit will be ignored while CR24 bit-1 is low.***
4	R/W	Serial flash interface configuration register.**(VBAT)** = 0 Normal mode. = 1 Fast mode. ***Note: The bit will be ignored while CR24 bit-1 is low.***
3~2	Reserved.	
1	R / W	PIN89, PIN90 function select (I^2C interafce) = 0 {PIN89, PIN90} → set by CR2C[6:5]. = 1 {PIN89, PIN90} → SDA, SCL.
0	R / W	KB, MS pin function select = 0 KB, MS function. = 1 GPIO function.

CR 2Bh. (Reserved)

CR 2Ch. (GPIO3, GPIO4 multi-function selection; Default 00h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	PIN88 Select = 0 PIN88→ GP34 = 1 PIN88→ RSTOUT4#
6	R / W	PIN89 Select = 0 PIN89→ GP33 = 1 PIN89→ RSTOUT3# ***Note: The bit will be ignored while CR2A bit-1 is High.***
5	R / W	PIN90 Select = 0 PIN90→ GP32 = 1 PIN90→ RSTOUT2# ***Note: The bit will be ignored while CR2A bit-1 is High.***
4	Reserved	
3	R / W	EN_VRM10 Configure bit = 0 VID input voltage is TTL. = 1 VID input voltage is VRM10. The bit is strapping by PIN77 (GP50).--- Pull high to 3VSB.

Continued.

BIT	READ / WRITE	DESCRIPTION
2	R / W	EN_PWRDN. **(VBAT)** = 0 Thermal shutdown function is disabled. = 1 Enable thermal shutdown function.
1~0	R / W	PIN78~85 function select

Bit-1	Bit-0	PIN78~PIN85 function
0	0	PIN82 → Reserved (tri-state) PIN83 → Reserved (always low) Others → GPIO4
0	1	PIN82 → IRRX PIN83 → IRTX Others → GPIO4
1	0	PIN 78~85 → GPIO4
1	1	PIN 78~85 → UART B

CR 2Dh. (GPIO5 and power control signals multi-function selection; default 21h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7	R / W	PIN67 Select (reset by RSMRST#) = 0 PIN67→ PSOUT# = 1 PIN67→ GPIO57
6	R / W	PIN68 Select (reset by RSMRST#) = 0 PIN68→ PSIN = 1 PIN68→ GPIO56
5	R / W	PIN70 Select (reset by RSMRST#) = 0 PIN70→ SUSLED = 1 PIN70→ GPIO55
4	R / W	PIN71 Select (reset by RSMRST#) = 0 PIN71→ PWROK = 1 PIN71→ GPIO54
3	R / W	PIN72 Select (reset by RSMRST#) = 0 PIN72→ PSON# = 1 PIN72→ GPIO53
2	R / W	PIN73 Select (reset by RSMRST#) = 0 PIN73→ SUSB# = 1 PIN73→ GPIO52

Continued.

BIT	READ / WRITE	DESCRIPTION
1	R / W	PIN75 Select (reset by RSMRST#) = 0 PIN75→ RSMRST# = 1 PIN75→ GPIO51
0	R / W	PIN77 Select (reset by RSMRST#) = 0 PIN77→ WDTO# = 1 PIN77→ GPIO50

CR 2Eh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Winbond.

CR 2Fh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Winbond.

7.2 Logical Device 0 (FDC)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h,F0h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select FDC I/O base address <100h : FF8h> on 8 bytes boundary.

CR 70h. (Default 06h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for FDC.

CR 74h. (Default 02h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for FDC. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 8Eh)

BIT	READ / WRITE	DESCRIPTION
7	R / W	This bit controls the internal pull-up resistors of the FDC input pins RDATA#, INDEX#, TRAK0#, DSKCHG# and WP#. 0: The internal pull-up resistors of FDC are turned on. 1: The internal pull-up resistors of FDC are turned off. (Default)
6	R / W	This bit determines the polarity of all FDD interface signals. 0: FDD interface signals are active low. 1: FDD interface signals are active high.
5	R / W	When this bit is logic 0, indicates a second drive is installed and is reflected in status register A. (PS2 mode only)
4	R / W	Swap Drive 0, 1 Mode => 0: No Swap. 1: Drive and Motor select 0 and 1 are swapped.
3~2	R / W	Interface Mode. 00: Model 30. 01: PS/2. 10: Reserved. 11: AT Mode
1	R / W	FDC DMA Mode. 0: Burst Mode is enabled 1: Non-Burst Mode.
0	R / W	Floppy Mode. 0: Normal Floppy Mode. 1: Enhanced 3-mode FDD.

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Boot Floppy. 00: FDD A. 01: FDD B. 10: FDD C. 11: FDD D.
5~4	R / W	Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.
3~2	R / W	Density Select. 00: Normal. 01 Normal. 10: 1 (Forced to logic 1). 11: 0 (Forced to logic 0).

Continued.

BIT	READ / WRITE	DESCRIPTION
1	R / W	DISFDDWR => 0: Enable FDD write. 1: Disable FDD write (forces pins WE, WD stay high).
0	R / W	SWWP => 0: Normal, use WP to determine whether the FDD is write protected or not. 1: FDD is always write-protected.

CR F2h. (Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	FDD D Drive Type.
5~4	R / W	FDD C Drive Type.
3~2	R / W	FDD B Drive Type.
1~0	R / W	FDD A Drive Type.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable FDC Pre-compensation. 1: Disable FDC Pre-compensation.
5	Reserved.	
4~3	R / W	Data Rate Table selection (Refer to TABLE A). 00: Select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 Meg Tape. 11: Reserved.
2	Reserved.	
1~0	R / W	Drive Type selection (Refer to TABLE B).

CR F5h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Same as FDD0 of CR F5h.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0 (PIN 2)	DRVDEN1 (PIN 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

7.3 Logical Device 1 (Parallel Port)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h, 78h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select PRT I/O base address. <100h : FFCh> on 4 bytes boundary (EPP not supported) or <100h : FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h. (Default 07h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PRT.

CR 74h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 3Fh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~3	R / W	ECP FIFO Threshold.
2~0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). 000: Standard and Bi-direction (SPP) mode. 001: EPP – 1.9 and SPP mode. 010: ECP mode. 011: ECP and EPP – 1.9 mode. 100: Printer Mode. 101: EPP – 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP – 1.7 mode.

7.4 Logical Device 2 (UART A)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h : FF8h> on 8 bytes boundary.

CR 70h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1~0	R / W	00: UART A clock source is 1.8462 MHz (24 MHz / 13). 01: UART A clock source is 2 MHz (24 MHz / 12). 10: UART A clock source is 24 MHz (24 MHz / 1). 11: UART A clock source is 14.769 MHz (24 MHz / 1.625).

7.5 Logical Device 3 (UART B)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 02h, F8h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 2 I/O base address <100h : FF8h> on 8 bytes boundary.

CR 70h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 2.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: No reception delay when SIR is changed from TX mode to RX mode. 1: Reception delay 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.
2	R / W	0: No transmission delay when SIR is changed from RX mode to TX mode. 1: Transmission delay 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.
1~0	R / W	00: UART B clock source is 1.8462 MHz (24 MHz / 13). 01: UART B clock source is 2 MHz (24 MHz / 12). 10: UART B clock source is 24 MHz (24 MHz / 1). 11: UART B clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: Through SINB / SOUTB. 1: Through IRRX / IRTX.
5~3	R / W	IRMODE => IR function mode selection. See below table.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: SOUTB pin of UART B function or IRTX pin of IR function in normal condition. 1: Inverse SOUTB pin of UART B function or IRTX pin of IR function.
0	R / W	0: SINB pin of UART B function or IRRX pin of IR function in normal condition. 1: Inverse SINB pin of UART B function or IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

7.6 Logical Device 5 (Keyboard Controller)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 00h,60h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the first KBC I/O base address <100h : FFFh> on 1 byte boundary.

CR 62h, 63h. (Default 00h,64h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the second KBC I/O base address <100h : FFFh> on 1 byte boundary.

CR 70h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h. (Default 0Ch)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h. (Default83h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	KBC clock rate selection 00: 6MHz 01: 8MHz 10: 12MHz 11: 16MHz
5~3	Reserved.	

Continued.

BIT	READ / WRITE	DESCRIPTION
2	R / W	0: Port 92 disable. 1: Port 92 enable.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST software control. 1: KBRST hardware speed up.

7.7 Logical Device 6 (Serial Flash Interface)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
1	R / W	0: Serial Flash Interface is inactive. 1: Activate Serial Flash Interface.
0	Reserved.	

CR 62h, 63h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Flash Interface I/O base address <100h : FF8h> on 1 byte boundary.

7.8 Logical Device 7 (GPIO1, GPIO6, Game Port & MIDI Port)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION	
7~4	Reserved.		
3	R / W	0: GPIO6 is inactive.	1: Activate GPIO6.
2	R / W	0: MIDI Port is inactive.	1: Activate MIDI Port.
1	R / W	0: Game Port is inactive.	1: Activate Game Port.
0	R / W	0: GPIO1 is inactive.	1: Activate GPIO1.

CR 60h, 61h. (Default 02h, 01h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Game Port base address <100h : FFFh> on 1 byte boundary.

CR 62h, 63h. (Default 03h, 30h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select MIDI Port base address <100h : FFEh> on 2 bytes boundary.

CR 70h. (Default 09h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MIDI Port.

CR F0h. (GPIO1 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an Output port 1: The respective GPIO1 PIN is programmed as an Input port.

CR F1h. (GPIO1 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. (GPIO1 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. (GPIO1 I/O register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → PLED
6	R / W	0: GPIO16 1: GPIO16 → WDTO#
5	R / W	0: GPIO15 1: GPIO15 → PLED
4	R / W	0: GPIO14 1: GPIO14 → WDTO#
3	R / W	0: GPIO13 1: GPIO13 → PLED
2	R / W	0: GPIO12 1: GPIO12 → WDTO#
1	R / W	0: GPIO11 1: GPIO11 → PLED
0	R / W	0: GPIO10 1: GPIO10 → WDTO#

CR F4h. (GPIO6 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an Output port 1: The respective GPIO6 PIN is programmed as an Input port.

CR F5h. (GPIO6 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. (GPIO6 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. (Game Port PAD control register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	Joystick Power Down 0: Joystick Power Down Disable. 1: Joystick Power Down Enable.

7.9 Logical Device 8 (WDTO# & PLED)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: WDTO# is inactive. 1: Activate WDTO#.

CR F5h. (WDTO#, PLED and KBC P20 control mode register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Select Power LED mode. 00: Power LED pin is tri-stated. 01: Power LED pin is driven low. 10: Power LED pin outputs 1Hz pulse with 50% duty cycle. 11: Power LED pin outputs $^1/_4$Hz pulse with 50% duty cycle.
5	Reserved.	
4	R / W	Faster 1000 times for WDTO# count mode. 0: Disable. 1: Enable. (If bit-3 is Second Mode , the count mode be 1/1000 Sec.) (If bit-3 is Minute Mode , the count mode be 1/1000 Min.)
3	R / W	Select WDTO# count mode. 0: Second Mode. 1: Minute Mode.
2	R / W	Enable the rising edge of KBC reset (P20) to issue time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the WDTO# output low pulse to the KBRST# pin (PIN60) 0: Disable. 1: Enable.
0	Reserved.	

CR F6h. (WDTO# counter register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. If the bit 7 and 6 of CR F7h are set, any Mouse Interrupt or Keyboard Interrupt event will also cause the reload of previously-loaded non-zero value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after 1 second/minute 02h: Time-out occurs after 2 second/minutes 03h: Time-out occurs after 3 second/minutes …… FFh: Time-out occurs after 255 second/minutes

CR F7h. (WDTO# control & status register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset watch-dog timer enable 0: Watchdog timer is not affected by mouse interrupt. 1: Watchdog timer is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset watch-dog timer enable 0: Watchdog timer is not affected by keyboard interrupt. 1: Watchdog timer is reset by keyboard interrupt.
5	Write “1” Only	Trigger WDTO# event. This bit is self-clearing.
4	R / W	WDTO# status bit 0: Watchdog timer is running. 1: Watchdog timer issues time-out event.
3~0	R / W	These bits select IRQ resource for WDTO#. (02h for SMI# event.)

7.10 Logical Device 9 (GPIO2,GPIO3, GPIO4, GPIO5 & SUSLED) (VSB Power)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION	
7~4	Reserved.		
3	R / W	0: GPIO5 is inactive.	1: Activate GPIO5
2	R / W	0: GPIO4 is inactive.	1: Activate GPIO4.
1	R / W	0: GPIO3 is inactive.	1: Activate GPIO3.
0	R / W	0: GPIO2 is inactive.	1: Activate GPIO2.

CR E0h. (GPIO5 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an Output port 1: The respective GPIO5 PIN is programmed as an Input port.

CR E1h. (GPIO5 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. (GPIO5 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. (GPIO2 register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an Output port 1: The respective GPIO2 PIN is programmed as an Input port

CR E4h. (GPIO2 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E5h. (GPIO2 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F0h. (GPIO3 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an Output port 1: The respective GPIO3 PIN is programmed as an Input port.

CR F1h. (GPIO3 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. (GPIO3 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. (Suspend LED mode register; Default 00h) **(VBAT power)**

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Select Suspend LED mode. 00: Suspend LED pin is tri-stated. 01: Suspend LED pin is driven low. 10: Suspend LED pin outputs 1Hz pulse with 50% duty cycle. 11: Suspend LED pin outputs $^1/_4$Hz pulse with 50% duty cycle.
5~0	Reserved.	

CR F4h. (GPIO4 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an Output port 1: The respective GPIO4 PIN is programmed as an Input port.

CR F5h. (GPIO4 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. (GPIO4 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. (GPIO4 multi-function select register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → SUSLED
6	R / W	0: GPIO46 1: GPIO46 → WDTO#
5	R / W	0: GPIO45 1: GPIO45 → SUSLED
4	R / W	0: GPIO44 1: GPIO44 → WDTO#
3	R / W	0: GPIO43 1: GPIO43 → SUSLED
2	R / W	0: GPIO42 1: GPIO42 → WDTO#
1	R / W	0: GPIO41 1: GPIO41 → SUSLED
0	R / W	0: GPIO40 1: GPIO40 → WDTO#

7.11 7.10 Logical Device A (ACPI)

(CR30, CR70 are VCC powered; CRE0~F7 are VRTC powered)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PME#.

CR E0h. (Default 01h) (VBAT power)

BIT	READ / WRITE	DESCRIPTION
7	R / W	DIS_PSIN => Disable panel switch input to turn system power supply on. 0: PSIN is wire-AND and connected to PSOUT#. 1: PSIN is blocked and cannot affect PSOUT#.
6	R / W	Enable KBC wake-up 0: Disable keyboard wake-up function via PSOUT#. 1: Enable keyboard wake-up function via PSOUT#.
5	R / W	Enable Mouse wake-up 0: Disable mouse wake-up function via PSOUT#. 1: Enable mouse wake-up function via PSOUT#.
4	R / W	MSRKEY => 3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the following table for the detailed.

ENMDAT_UP	MSRKEY	MSXKEY	Wake-up event
1	x	1	Any button clicked or movement.
1	x	0	One click of either left or right MS button.
0	0	1	One click of the MS left button.
0	1	1	One click of the MS right button.
0	0	0	Two clicks of the MS left button.
0	1	0	Two clicks of the MS right button.

Continued.

BIT	READ / WRITE	DESCRIPTION
3	Reserved.	
2	R / W	Keyboard / Mouse swap enable 0: Normal mode. 1: Keyboard / Mouse ports are swapped.
1	R / W	MSXKEY => 3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.
0	R / W	KBXKEY => 0: Only the pre-determined key combination in sequence can wake up the system. 1: Any character received from keyboard can wake up the system.

CR E1h. (KBC Wake-Up Index Register; Default 00h) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up index register. It is the index register of CRE2, which is the access window of keyboard pre-determined key combination characters. The first set of wake up key combination is in the range of 0x00 - 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combination can be read through 0x10 – 0x1E.

CR E2h. (KBC Wake-Up Data Register; Default ffh) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up data register. It is the data register of the keyboard pre-determined key combination characters, which is indexed by CRE1.

CR E3h. (Event Status Register; Default 08h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	Read Only Read-Clear	This event status is caused by VSB power off/on.
4	Read Only Read-Clear	If E4[7] is 1 => This bit is 0: When power-loss occurs and VSB power is on, indicate that turn on system power. This bit is 1: When power-loss occurs and VSB power is on, indicate that turn off system power. If E4[7] is 0 => This bit is always 0.

Continued.

BIT	READ / WRITE	DESCRIPTION
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: The thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: The PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: The mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: The keyboard wake-up event issued.

CR E4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Power loss control bit 2 0： Indicates that PSON#（Pin 72）outputs logic low after PSOUT# issues a low pulse. 1： Indicates that PWRCTL# will output logic low after resume from AC power loss if SUSB#（Pin 73）is logic high.
6~5	R / W	Power loss control bits <1：0> => (**VBAT**) 00: System always turns off when come back from power loss state. 01: System always turns on when come back from power loss state. 10: System turns off / on when come back from power loss state depend on the state before power loss. 11: User define the state before power loss.(The last state set at CRE6[4])
4	Reserved	
3	R / W	Keyboard wake-up options. **(LRESET#)** 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for all wake-up events set in CRE0. This bit is cleared when any wake-up events is captured. **(LRESET#)** 0: Disable. 1: Enable.
1~0	Reserved.	

CR E5h. (Reserved)

BIT	READ / WRITE	DESCRIPTION
7~0	Reserved.	

CR E6h. (Default 1Ch)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => **(VSB)** 3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.
6	Reserved.	
5	R / W	CASEOPEN Clear Control. **(VSB)** Write 1 to this bit will clear CASEOPEN status. This bit won't be self cleared, please write 0 after event be cleared. The function is as same as Index 46h bit 7 of H/W Monitor part.
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF.
3	R / W	PWROK_DEL (first stage) **(VSB)** Set the delay rising time from PWROK_LP to PWROK_ST. 0: 300 ~ 600 ms. 1: 200 ~ 300 ms.
2~1	R / W	PWROK_DEL **(VSB)** Set the delay rising time from PWROK_ST to POWEROK. 00: No delay time. 01: Delay 32 ms 10: 96 ms 11: Delay 250 ms
0	R / W-Clear	PWROK_TRIG => Write 1 to re-trigger POWEROK signals from low to high.

CR E7h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => **(VSB)** Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => **(VSB)** Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => **(VSB)** Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s long PSOUT# pulse when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (for SiS & VIA chipsets) 0: Disable. 1: Enable.
3	R / W	Select WDTO# reset source **(VSB)** 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by POWEROK
2~1	Reserved.	
0	R / W	Hardware Monitor RESET source select **(VBAT)** 0: POWEROK 1: LRESET#

CR E8h. (Reserved)

CR F2h. (Default 7Ch) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Enable RSTOUT4# function. 0: Disable RSTOUT4#. 1: Enable RSTOUT4#.
5	R / W	Enable RSTOUT3# function. 0: Disable RSTOUT3#. 1: Enable RSTOUT3#.
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#.
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#.
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#.
1	Reserved.	
0	R / W	EN_PME => 0: Disable PME. 1: Enable PME.

CR F3h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W-Clear	PME status of the Mouse IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the FDC IRQ event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDTO# event. Write 1 to clear this status.
1	R / W-Clear	PME status of the MIDI IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

CR F6h. (Default 00h) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	0: Disable PME interrupt of the Mouse IRQ event. 1: Enable PME interrupt of the Mouse IRQ event.
4	R / W	0: Disable PME interrupt of the KBC IRQ event. 1: Enable PME interrupt of the KBC IRQ event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	R / W	0: Disable PME interrupt of the FDC IRQ event. 1: Enable PME interrupt of the FDC IRQ event.
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

CR F7h. (Default 00h) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDTO# event. 1: Enable PME interrupt of the WDTO# event.
1	R / W	0: Disable PME interrupt of the MIDI IRQ event. 1: Enable PME interrupt of the MIDI IRQ event.
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

7.12 Logical Device B (Hardware Monitor, for W83627EHF/EHG only)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 00h, 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select HM base address <100h : FFEh> on 2 bytes boundary.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for HM.

CR F0h. (VID Control register; Default C1h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	VID I/O Control (CRF1[5:0]) 0: VID output mode. 1: VID input mode.
6-0	Reserved.	

CR F1h. (VID Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5~0	R / W	VID[5:0] Data Register.

8. SPECIFICATIONS

8.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (3.3V)	-0.5 to 6.5	V
Input Voltage	-0.5 to V_{DD}+0.5	V
RTC Battery Voltage V_{BAT}	2.2 to 4.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2 DC CHARACTERISTICS

(T_a = 0°C to 70°C, V_{DD} = 3.3V ± 10%, V_{SS} = 0V, V_{DD} is 5V± 10% tolerance)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	I_{BAT}			2.4	µA	V_{BAT} = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	I_{BAT}			2.0	mA	V_{SB} = 3.3 V, All ACPI pins are not connected.
I/O_{8t} - TTL level bi-directional pin with 8mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12t} - TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC CHARACTERISTICS, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{24t} - TTL level bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12ts} - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24ts} - TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}= 3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA

DC CHARACTERISTICS, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24tsp3} – 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12t} - TTL level bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24t} - TTL level bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V

DC CHARACTERISTICS, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
$I/OD12_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
$I/OD16_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 16mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

DC CHARACTERISTICS, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD12csd - CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Hystersis	VTH	0.5	1.2		V	VDD = 3.3 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Input High Leakage	ILIH			+10	μA	VIN = 3.3 V
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
I/OD12csu - CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	VDD = 3.3 V
Hystersis	VTH	0.5	1.2		V	VDD = 3.3 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Input High Leakage	ILIH			+10	μA	VIN = 3.3 V
Input Low Leakage	ILIL			-10	μA	VIN = 0 V
O4 - Output pin with 4mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 4 mA
Output High Voltage	VOH	2.4			V	IOH = -4 mA
O8 - Output pin with 8mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = -8 mA
O12 - Output pin with 12mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Output High Voltage	VOH	2.4			V	IOH = -12 mA
O16 - Output pin with 16mA source-sink capability						
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Output High Voltage	VOH	2.4			V	IOH = -16 mA

DC CHARACTERISTICS, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
O_{24} - Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} - 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24p3} - 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12} - Open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} - 3.3V open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tp3} - 3.3V TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{td} - TTL level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

DC CHARACTERISTICS, continued.

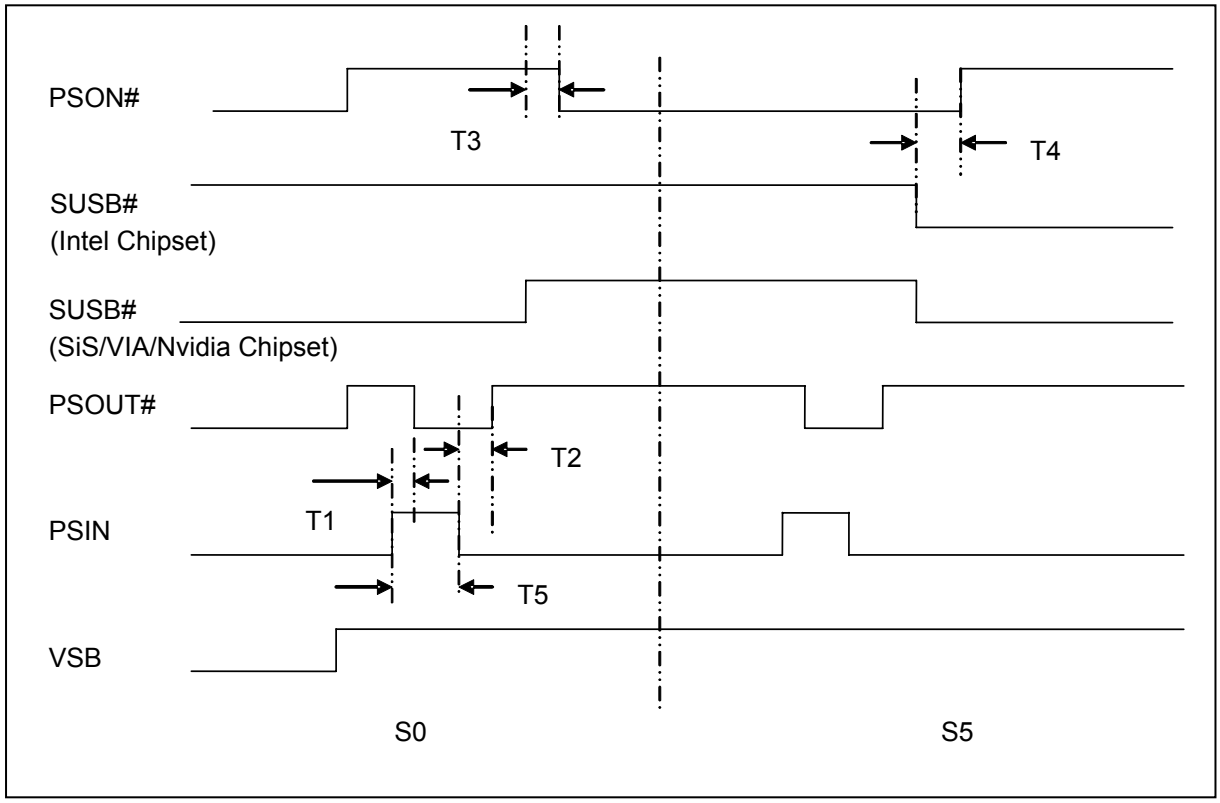
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{tu} - TTL level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp3} - 3.3 V TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{c} - CMOS level input pin						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{cd} - CMOS level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

DC CHARACTERISTICS, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{cs} - CMOS level Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 3.3V
Hystersis	VTH	1.5	2		V	V_{DD} = 3.3V
Input High Leakage	ILIH			+10	μA	V_{IN} = 3.3V
Input Low Leakage	ILIL			-10	μA	V_{IN} = 0 V
IN_{csu} - CMOS level Schmitt-trigger input pin with internal pull up resistor						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	V_{DD} = 3.3V
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	V_{DD} = 3.3V
Hystersis	VTH	0.5	1.2		V	V_{DD} = 3.3V
Input High Leakage	ILIH			+10	μA	V_{IN} = 3.3V
Input Low Leakage	ILIL			-10	μA	V_{IN} = 0 V

8.3 AC CHARACTERISTICS

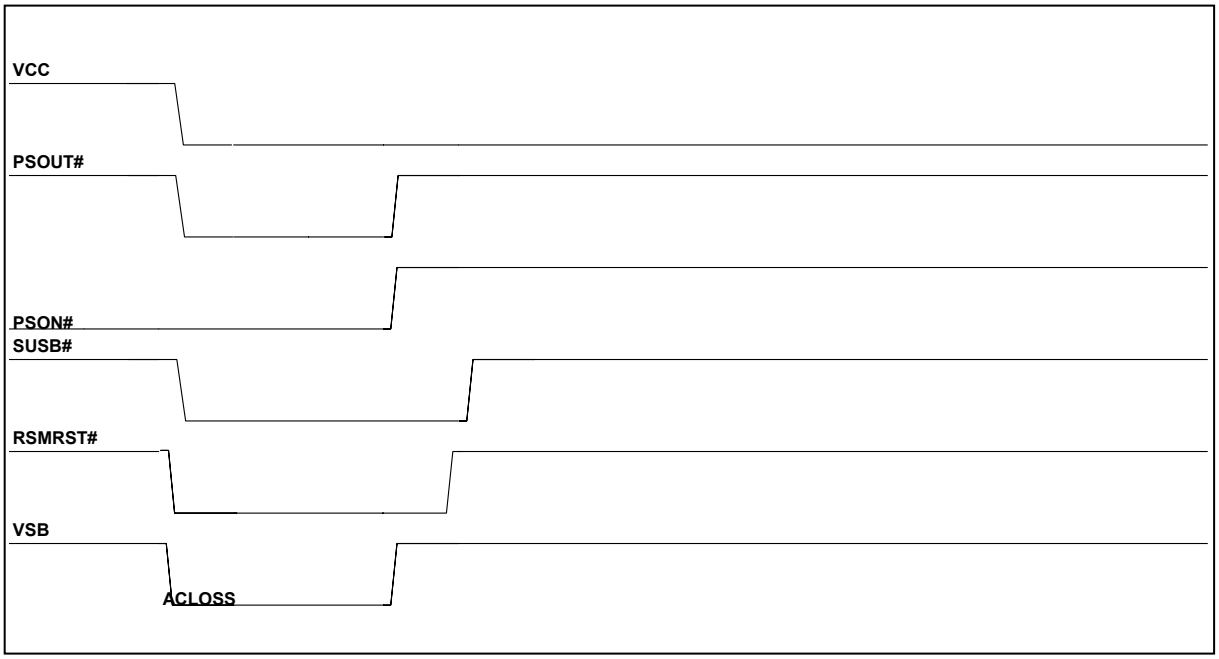
8.3.1 Power On / Off Timing



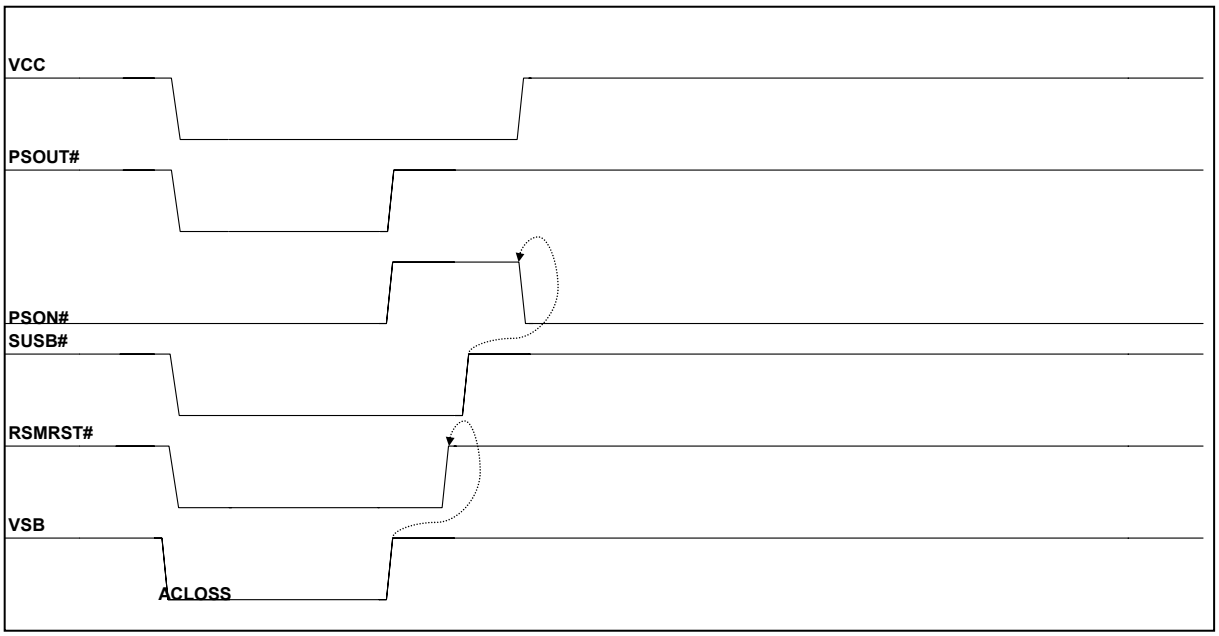
	T1	T2	T3	T4	T5
Typical Timing (Sec)	61m	0m	0m	21m	Over 64m at least

8.3.2 AC Power Failure Resume Timing

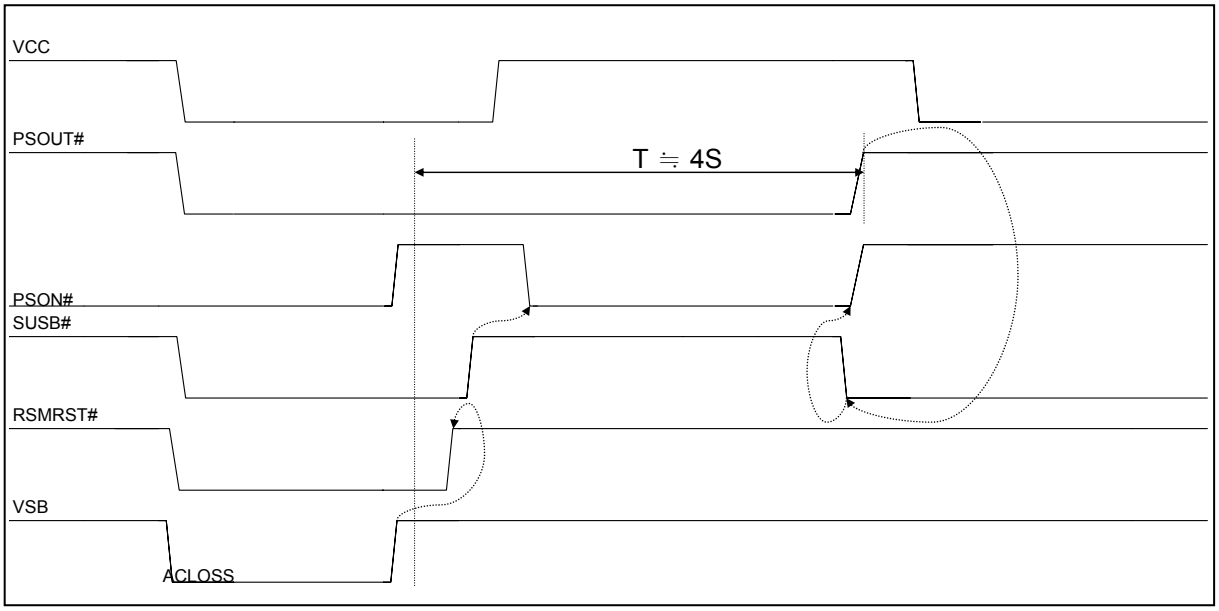
1. CRE4 bit7 = “0” and CRE4 bit[6:5] are selected to “OFF” state
   (“OFF” means always turn off or last state is off)



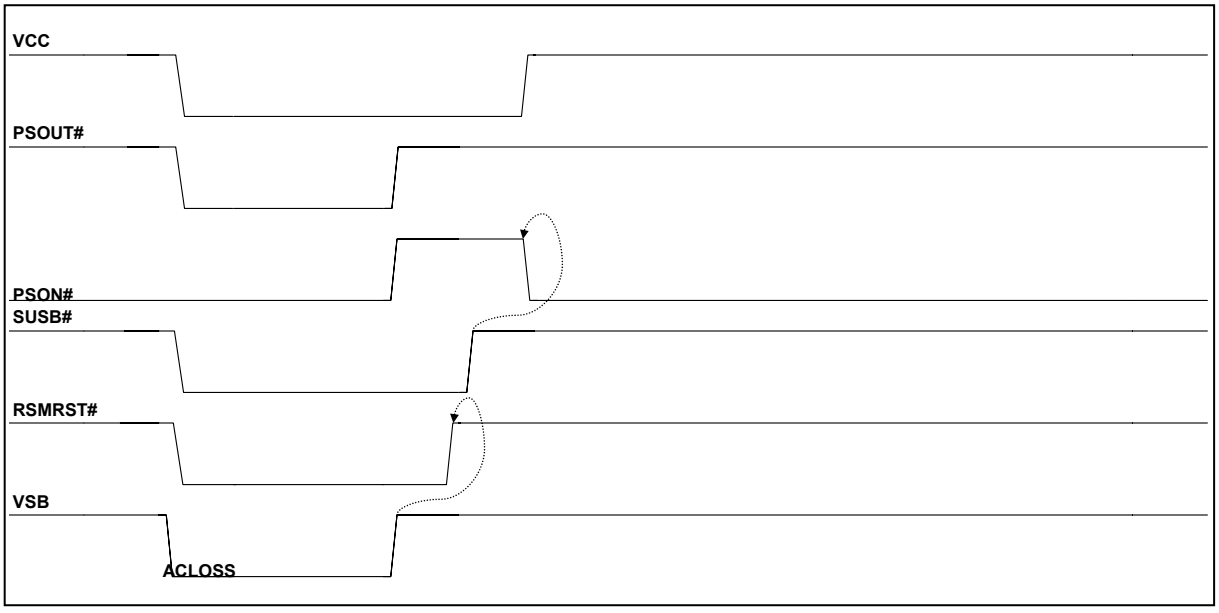
2. CRE4 bit7 = “0” and CRE4 bit[6:5] are selected to “ON” state
   (“ON” means always turn on or last state is on)



3. CRE4 bit7 = “1” and CRE4 bit[6:5] are selected to “OFF” state
(“OFF” means always turn off or last state is off)



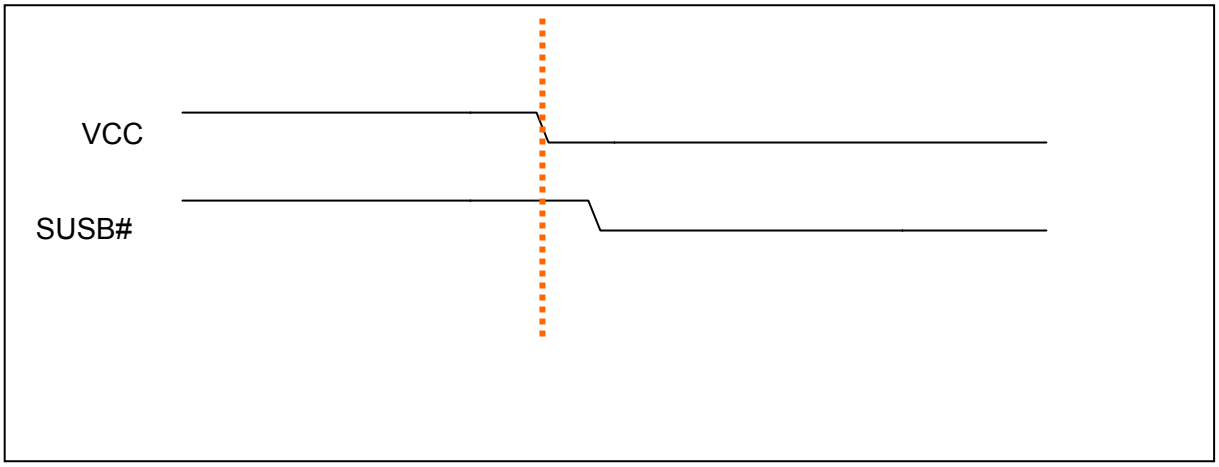
4. CRE4 bit7 = “1” and CRE4 bit[6:5] are selected to “ON” state
(“ON” means always turn on or last state is on)



**** What's the definition of last state when AC power failure?**

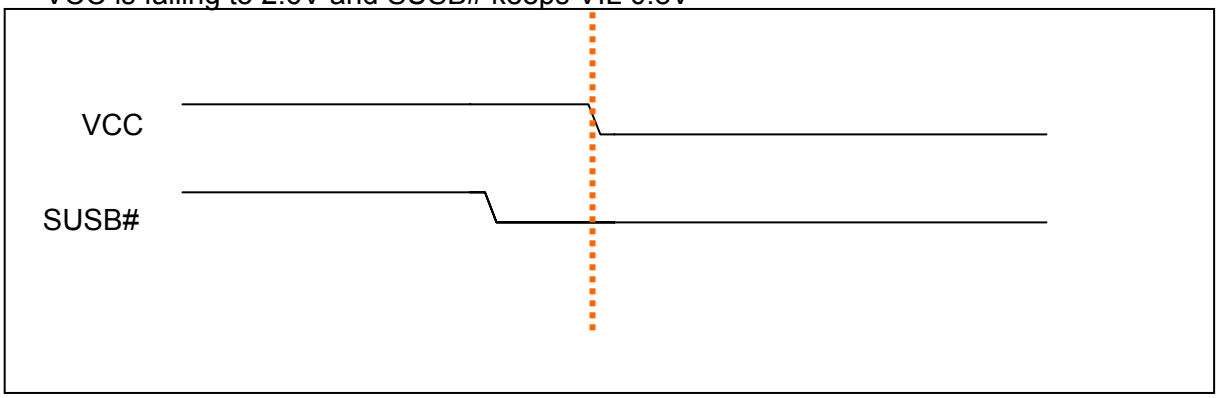
1) Last state is "ON"

VCC is falling to 2.6V and SUSB# keeps VIH 2.0V



2) Last state is "OFF"

VCC is falling to 2.6V and SUSB# keeps VIL 0.8V



To prevent that VCC goes down faster than VSB in various ATX Power Supply. W83627EHF/EF,W83627EHG/EG add the "user define mode" option for AC power loss pre-state. BIOS can set the pre-state that is "On" or "Off" state, because the status of AC power resume depends on it.

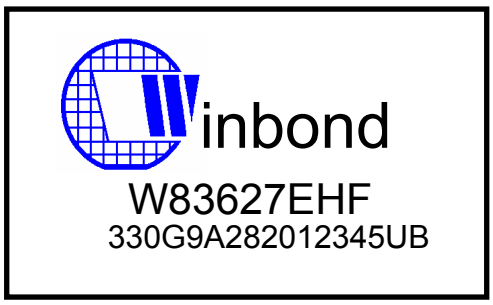
CR E4h

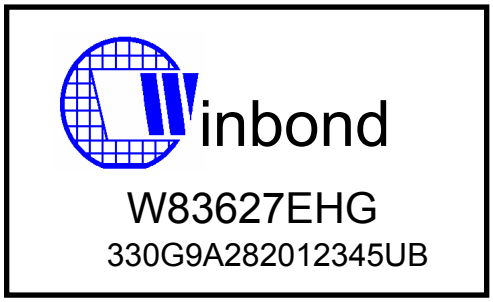
6~5	R / W	Power loss control bits => (**VBAT**) 00: System always turns off when come back from power loss state. 01: System always turns on when come back from power loss state. 10: System turns off / on when come back from power loss state depend on the state before power loss. 11: User define the state before power loss.(The last state set at CRE6[4])

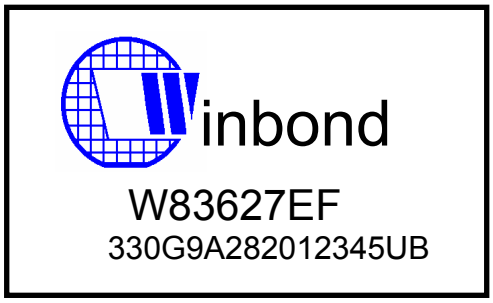
CR E6h

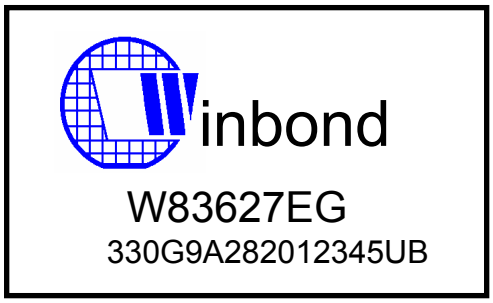
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

9. HOW TO READ THE TOP MARKING







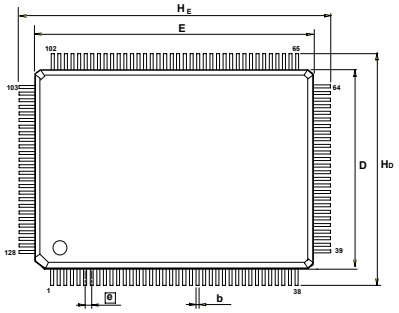


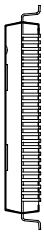
1st line: Winbond logo
2nd line: the type number: W83627EHF/EF, W83627EHG/EG (Pb-free package)
3rd line: the tracking code 030A7C282012345UA

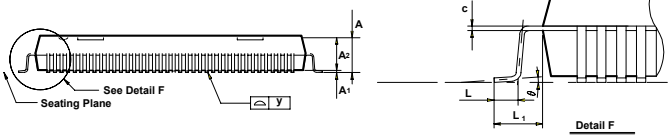
330: packages made in '03, week 30
G: assembly house ID; G means GR, A means ASE ... etc.
9: code version; 9 means code 009
A: IC revision; A means version A, B means version B
282012345: wafer production series lot number
UB: Winbond internal use.

10. PACKAGE SPECIFICATION

(128-pin PQFP)







Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

Important Notice

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