3A, Ultra-Low Dropout Voltage Regulator

General Description

The RT9059 is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 3A. It operates with a VIN as low as 1V and VDD voltage 3V with programmable output voltage as low as 0.8V. The RT9059 features ultra low dropout, ideal for applications where VOUT is very close to VIN. Additionally, it has an enable pin to further reduce power dissipation while shutdown. The RT9059 provides excellent regulation over variations in line, load and temperature. The RT9059 provides a power good signal to indicate if the voltage level of V_O reaches 90% of its rating value.

Features

- **Output Current up to 3A**
- **High Accuracy ADJ Voltage 1.5%**
- **Dropout Voltage 350mV @ 3A Typically**
- **VOUT Power Good Signal**
- **VOUT Pull Low Resistance when Disable**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook PC Applications
- Motherboard Applications

Ordering Information

RT9059(-□□)□□

Package Type
SP: SOP-8 (Exposed Pad-Option 1)
QW : WDFN-10L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

None : Adjustable Output
Fixed Output Voltage Code
15 : 1.5V
18 : 1.8V
25 : 2.5V

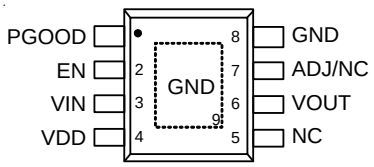
Note :

Richtek products are :

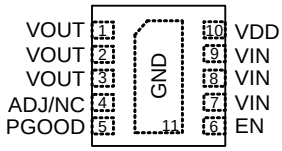
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

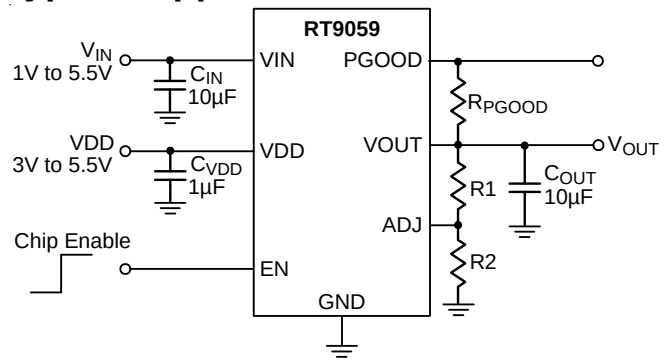


WDFN-10L 3x3

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit



V_{OUT} = 0.8 x (R1+R2)/R2

Figure 1. Adjustable Voltage Regulator

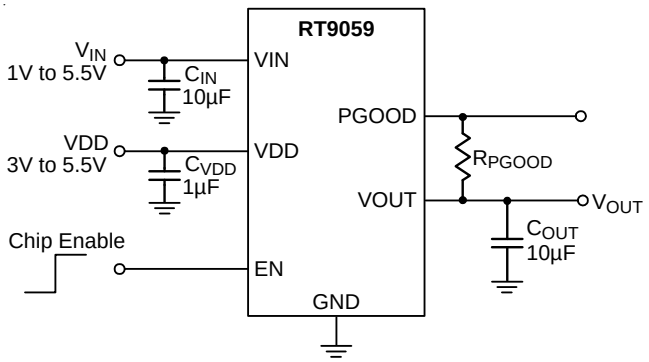
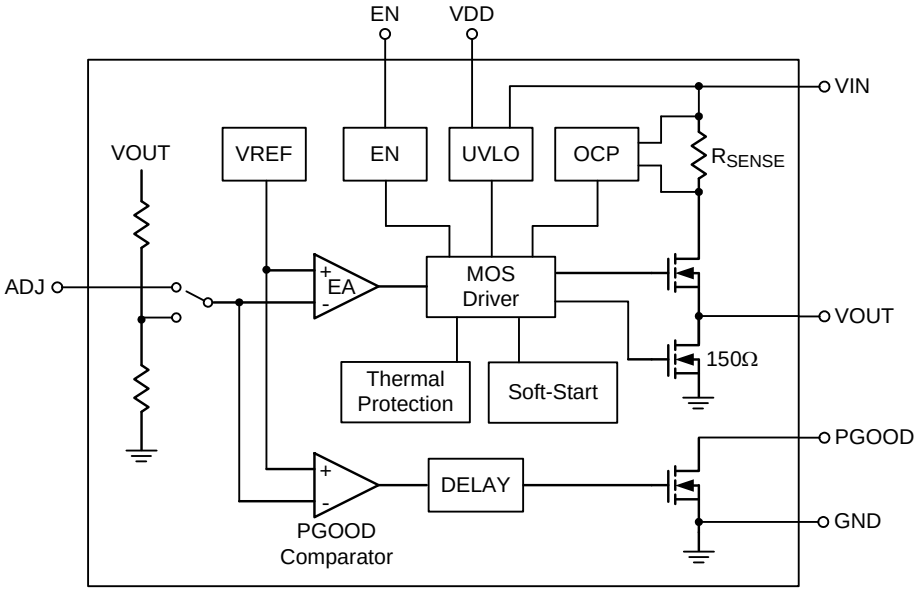


Figure 2. Fixed Voltage Regulator

Functional Pin Description

Pin No.				Pin Name	Pin Function
SOP-8 (Exposed Pad)		WDFN-10L 3x3			
Adjustable Output Voltage	Fixed Output Voltage	Adjustable Output Voltage	Fixed Output Voltage		
1	1	5	5	PGOOD	Power Good Open Drain Output.
2	2	6	6	EN	Enable Control Input.
3	3	7, 8. 9	7, 8. 9	VIN	Supply Input Voltage.
4	4	10	10	VDD	Supply Voltage of Control Circuit.
5	5, 7	--	4	NC	No Internal Connection.
6	6	1, 2, 3	1, 2, 3	VOUT	Output Voltage.
7	--	4	--	ADJ	Output Voltage Setting. $V_{OUT} = V_{REF}$ x (R1+R2)/R2.
8, 9 (Exposed Pad)	8, 9 (Exposed Pad)	11 (Exposed Pad)	11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN to GND
  - DC ---------- –0.3V to 6V
  - < 10ms ---------- –0.3V to 7V
- Control Voltage, VDD to GND
  - DC ---------- –0.3V to 6V
  - < 10ms ---------- –0.3V to 7V
- Output Voltage, VOUT ---------- –0.3V to 6V
- Chip Enable Voltage, EN ---------- –0.3V to 6V
- Adjust Voltage, ADJ ---------- –0.3V to 6V
- Power Good Voltage, V_{PGOOD} ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 (Exposed Pad) ---------- 2.96W
  - WDFN-10L 3x3 ---------- 2.95W
- Package Thermal Resistance (Note 2)
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 33.7°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 5.4°C/W
  - WDFN-10L 3x3, θ_{JA} ---------- 33.8°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 8.9°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 1V to 5.5V
- Control Voltage, VDD (V_{DD} > V_{OUT} + 1.5V) ---------- 3V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 5V, C_{IN} = C_{OUT} = 10µF, C_{VDD} = 1µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Operation Range	V_{DD}		3	--	5.5	V
VDD POR Threshold	V_{POR_VDD}	V_{DD} Rising	2.4	2.7	3	V
VDD POR Falling Hysteresis	ΔV_{POR_VDD}	V_{DD} Falling	0.15	0.2	--	V
Input Voltage Range	V_{IN}		1	--	5.5	V
VIN POR Threshold	V_{POR_VIN}	V_{IN} Rising	0.7	0.8	0.9	V
VIN POR Falling Hysteresis	ΔV_{POR_VIN}	V_{IN} Falling	0.15	0.2	0.25	V
Quiescent Current	I_Q	EN On, No Load	--	0.6	1.2	mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage		V_{REF}		0.788	0.8	0.812	V
Fixed Output Voltage Accuracy				–1.5	--	1.5	%
VOUT Load Regulation		ΔV_{LOAD}	I_{OUT} = 1mA to 3A, V_{IN} = V_{OUT}+1V	--	0.5	1	%
OUT Line Regulation		ΔV_{LINE}	V_{DD} = 3.6V to 5.5V, V_{IN} = V_{OUT}+1V to 5V, I_{OUT} = 1mA	--	0.2	0.6	%
Dropout Voltage		V_{DROP}	I_{OUT} = 2A	--	250	350	mV
			I_{OUT} = 3A	--	350	450	
Current Limit		I_{LIM}	V_{IN} = 3.6V	3.1	3.6	4.2	A
Short Circuit Current		I_{SC}	V_{OUT} < 0.2V	1	1.4	1.8	A
VOUT Pull Low Resistance		R_{PULL}	V_{EN} = 0V	--	150	--	Ω
Thermal Shutdown Temperature		T_{SD}		--	160	--	°C
Thermal Shutdown Recovery Temperature		T_{SDR}		--	90	--	°C
PGOOD Rising Threshold		V_{TH_PGOOD}	V_{OUT} Rising	--	90	--	%
PGOOD Hysteresis		ΔV_{TH_PGOOD}	V_{OUT} Falling	--	10	--	%
PGOOD Delay Time				--	1	1.5	ms
PGOOD Sink Capability		V_{PGOOD}	I_{SINK} = 10mA	--	0.2	0.4	V
EN Input Voltage	Logic-High	V_{IH}		1.2	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
EN Delay Time				0.3	0.85	1.4	ms
EN Pin Bias Current		I_{EN}	V_{EN} = 5V	--	12	--	μA
VDD Pin Shutdown Current		I_{SHDN_VDD}	V_{EN} = 0V	--	--	1	μA
VIN Pin Shutdown Current		I_{SHDN_VIN}	V_{EN} = 0V, V_{IN} = 5V	--	--	1	μA
Inrush Current		I_{INRUSH}	V_{OUT} = 1.8V, C_{OUT} = 10μF, I_{Load} = 1A	--	0.5	--	A
Soft-Start Time		t_{SS}		1.9	2.8	3.75	ms

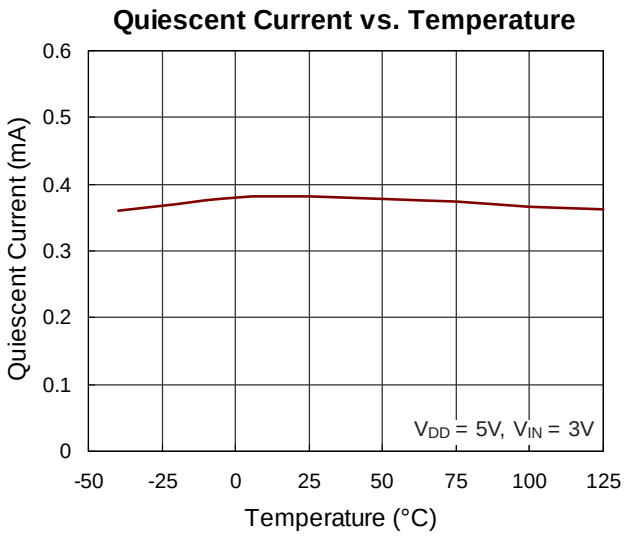
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

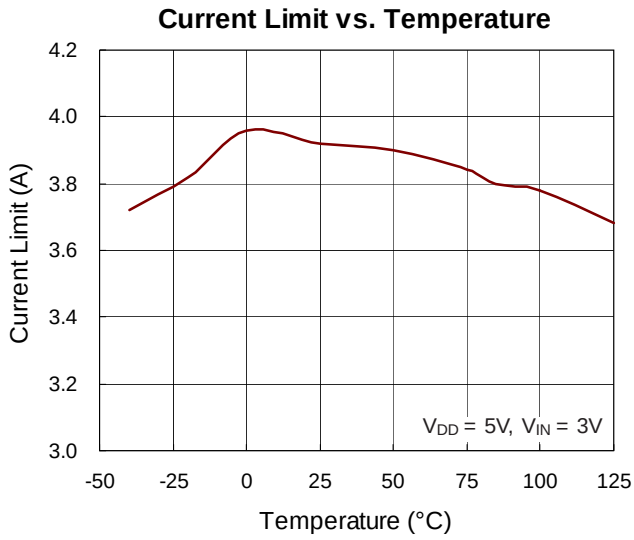
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

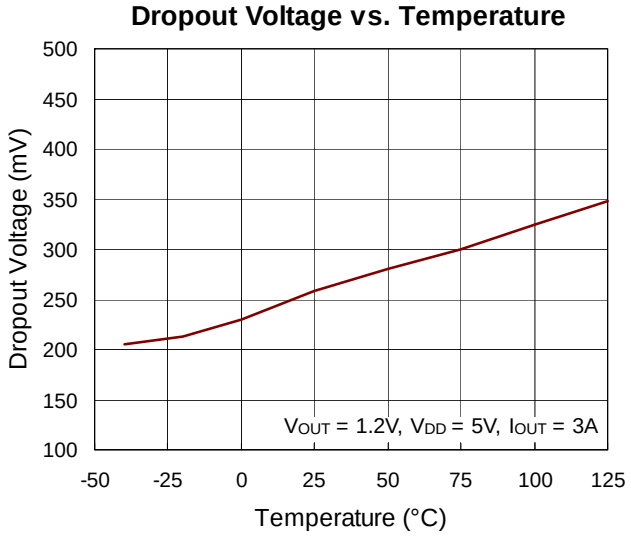
Note 3. Devices are ESD sensitive. Handling precaution recommended.

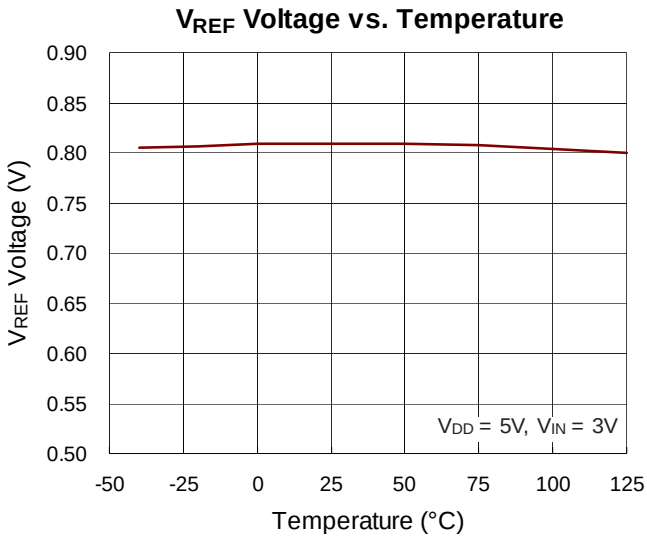
Note 4. The device is not guaranteed to function outside its operating conditions.

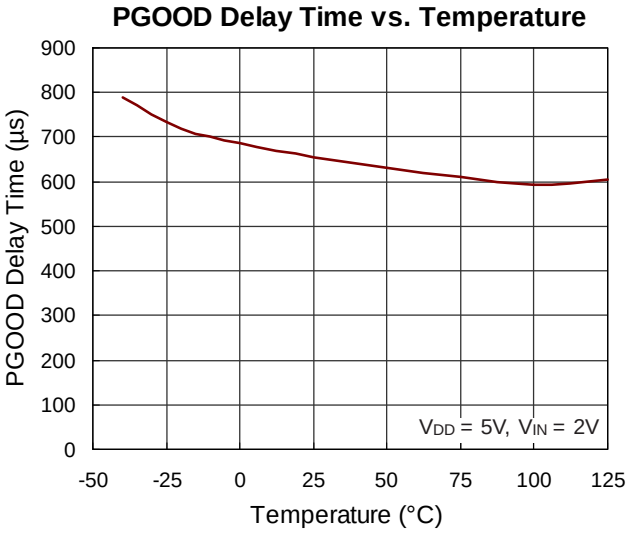
Typical Operating Characteristics

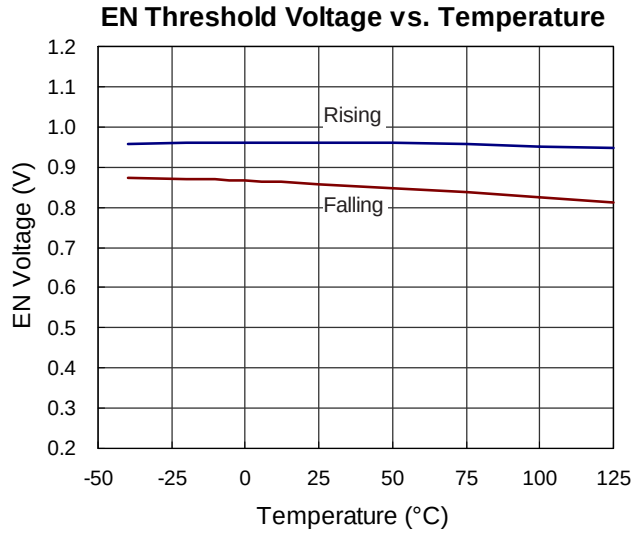




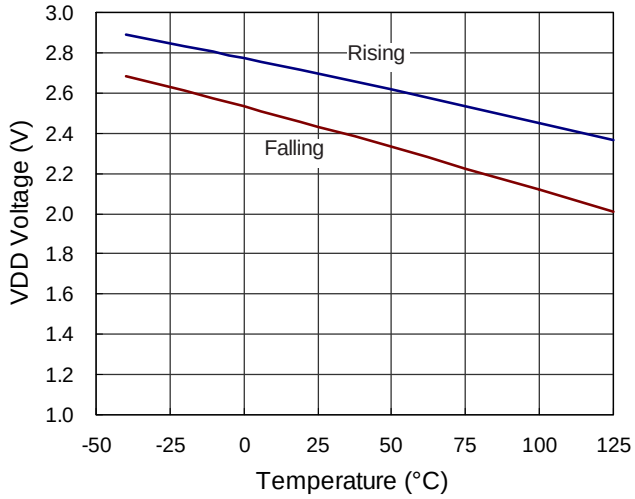




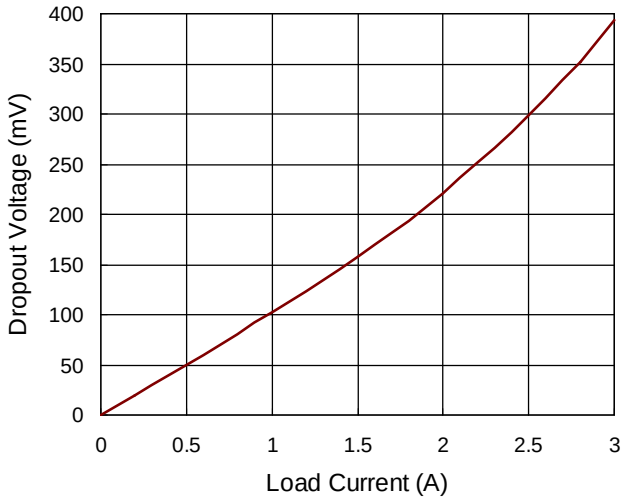




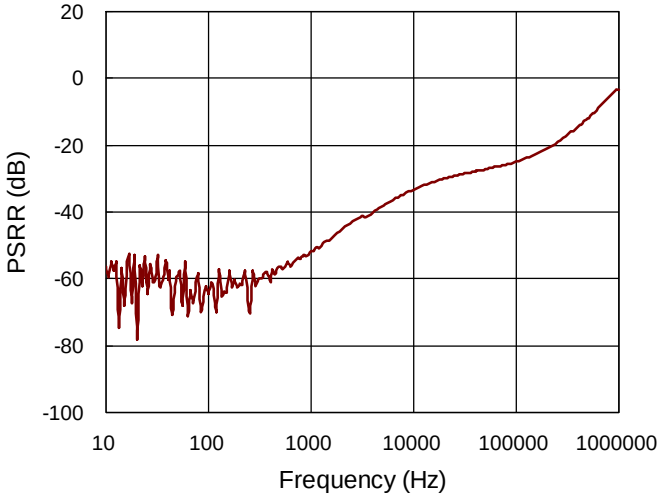
VDD POR Threshold Voltage vs. Temperature



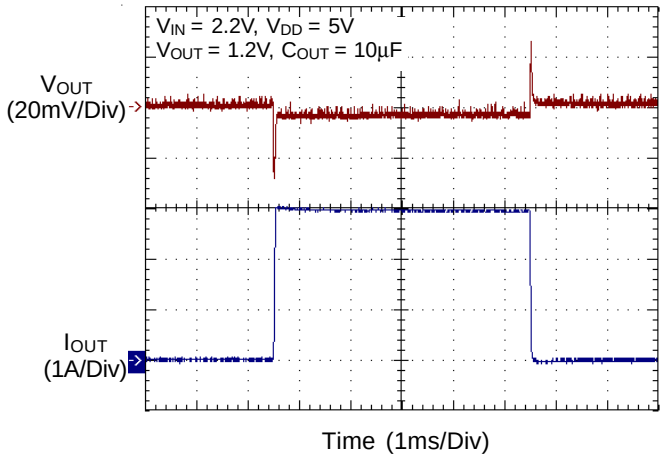
Dropout Voltage vs. Load Current



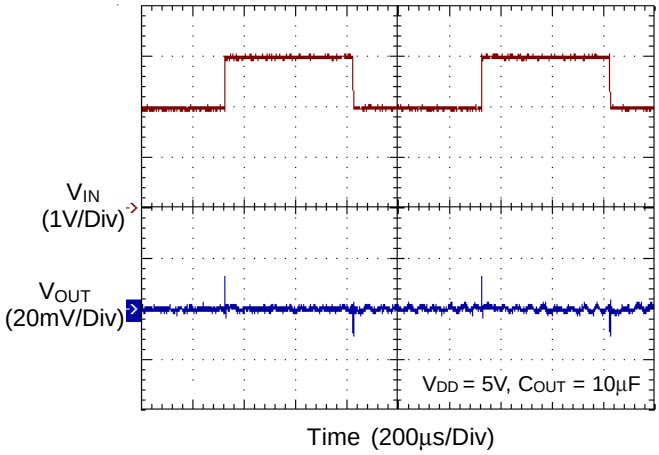
PSRR vs. Frequency



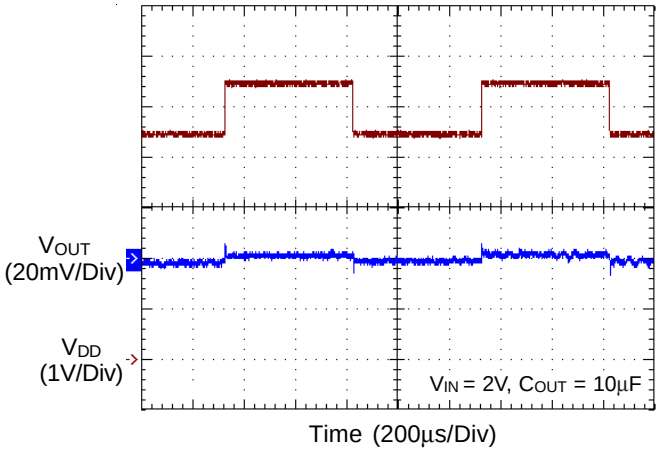
Load Transient Response



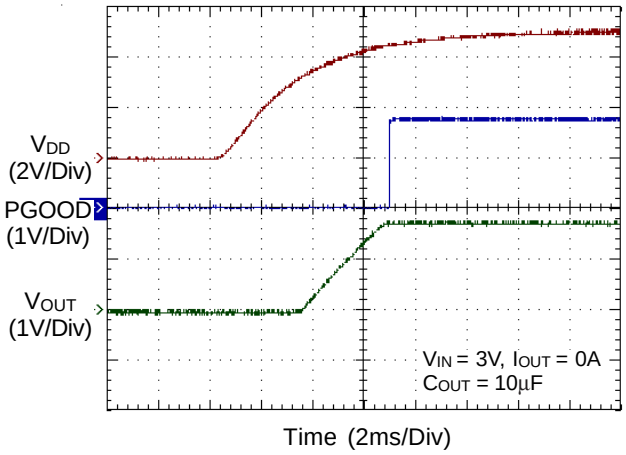
V_{IN} Line Transient Response



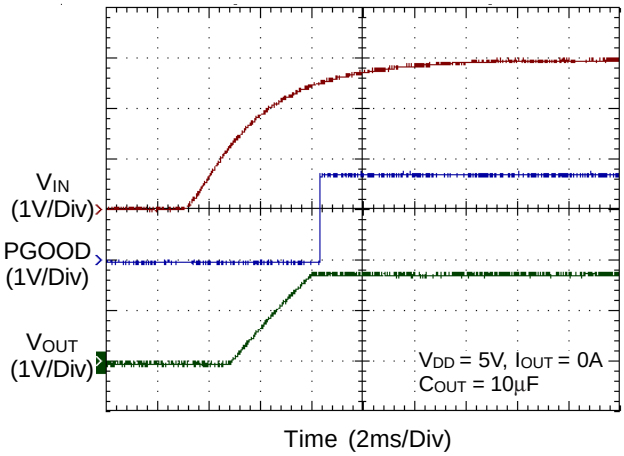
V_{DD} Line Transient Response



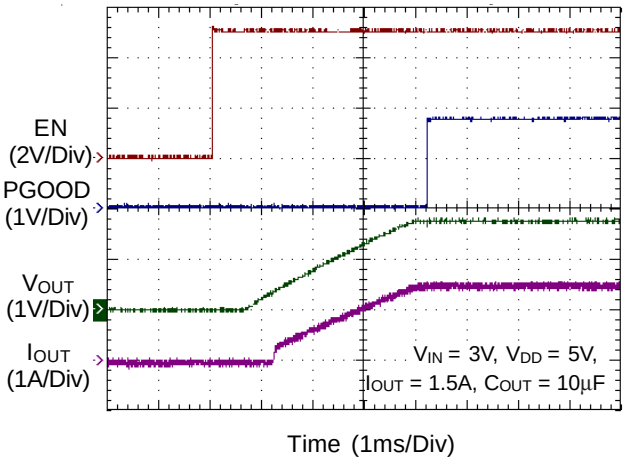
Start Up from V_{DD}



Start Up from V_{IN}



Start Up from Enable and PGOOD Delay



Applications Information

Adjustable Mode Operation

The output voltage of RT9059 is adjustable from 0.8V to VIN by external voltage divider resisters as shown in Typical Application Circuit (Figure 1). The value of resisters R1 and R2 should be more than 10kΩ to reduce the power loss. The output voltage can be calculated by the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the reference voltage (0.8V typical).

Enable

The RT9059 goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 1μA typical. The RT9059 goes into operation mode when the EN pin is in the logic high condition. If the EN pin is floating, please notice the RT9059 internal initial logic level. For RT9059, the EN pin function pulls low level internally. So the regulator will be turned off when EN pin is floating.

Input Capacitor

Good bypassing is recommended from input to ground to improve AC performance. A 10μF input capacitor or greater located as close as possible to the IC is recommended.

Output Capacitor

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9059 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor which value is at least 10μF on the RT9059 output ensures stability. The RT9059 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9059 and returned to a clean analog ground.

Current Limit

The RT9059 contains an independent current limit and the short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, minimum limiting the output current to 3.1A typical. When the output voltage is less than 0.2V, the short circuit current protection starts the current fold back function and maintains the loading current at maximum 1.8A. The output can be shorted to ground indefinitely without damaging the part.

Power Good

The power good function is an open-drain output. Connect 100kΩ pull up resistor to V_{OUT} to obtain an output voltage. The PGOOD pin will output high immediately after the output voltage arrives 90% of normal output voltage.

Thermal Shutdown Protection

Thermal protection limits power dissipation to prevent IC over temperature in RT9059. When the operation junction temperature exceeds 160°C, the over temperature protection circuit starts the thermal shutdown function and turns the pass transistor off. The pass transistor turns on again after the junction temperature cools by 70°C.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 33.7°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 33.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (33.7°C/W) = 2.96W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (33.8°C/W) = 2.95W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

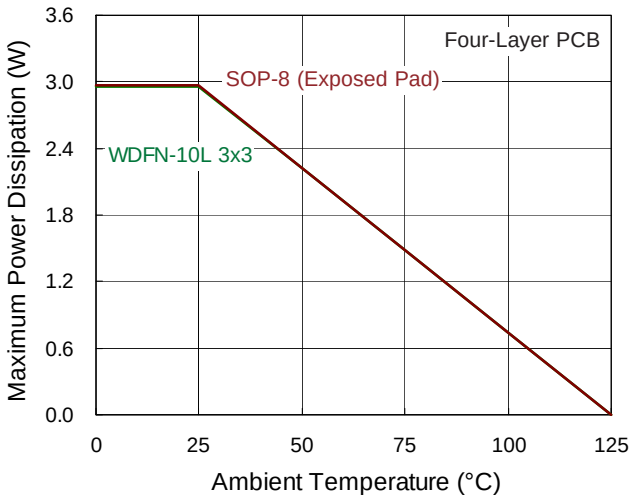
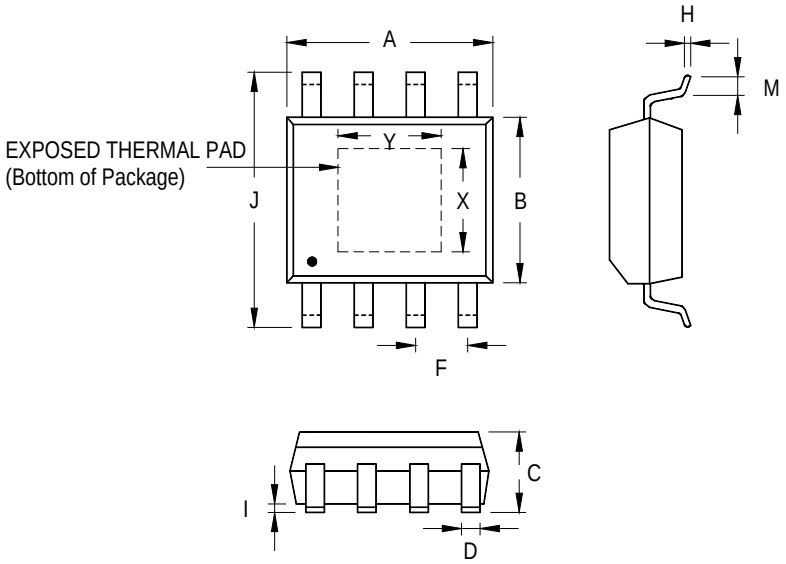


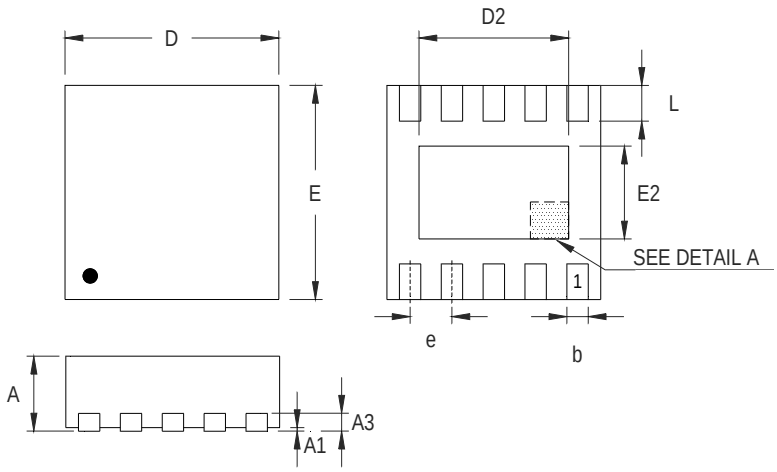
Figure 3. Derating Curve of Maximum Power Dissipation

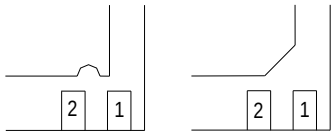
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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