Dual 8-Bit Buffered Multiplying CMOS D/A Converter

T-51-09-08 **PM-7528**

2

FEATURES

- On-Chip Latches For Both DACs
- +5V To +15V Single Supply Operation
- DACs Matched To 1%
- Four-Quadrant Multiplication
- TTL/CMOS Compatible
- 8-Bit Endpoint Linearity (±1/2 LSB)
- Full Temperature Operation
- Low Power Consumption
- Microprocessor Compatible
- Improved ESD Resistance
- Automatically Insertable Cerdip and Plastic Packages
- Available In Surface Mount SO, PLCC and LCC Packages
- Available In Die Form

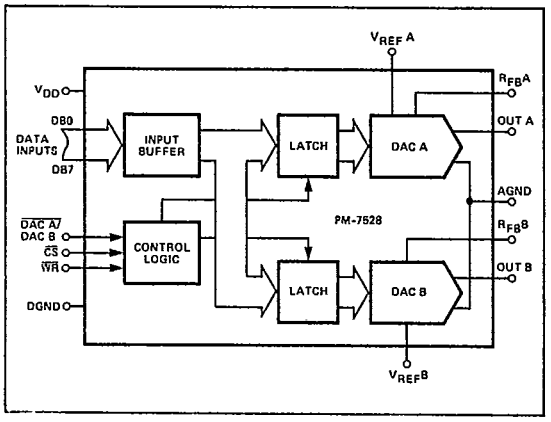
APPLICATIONS

- Digital Gain/Attenuation Control
- Digital Control Of Filter Parameters
- Digitally-Controlled Audio Circuits
- X-Y Graphics
- Digital/Synchro Conversion
- Robotics
- Ideal For Battery-Operated Equipment

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7528AR	AD7528UD	MIL
PM7528BR	AD7528TD	
PM7528BR	AD7528SD	
PM7528ER	AD7528CQ	IND
PM7528FR	AD7528BQ	
PM7528FR	AD7528AQ	
PM7528GP	PM7528GP	COM
PM7528FP	AD7528LN	
PM7528FPC	AD7528KP	

FUNCTIONAL DIAGRAM



ORDERING INFORMATION †

RELATIVE ACCURACY	GAIN ERROR	PACKAGE: MILITARY* TEMPERATURE −55°C TO +125°C	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE −40°C TO +85°C	PACKAGE: COMMERCIAL TEMPERATURE 0°C TO +70°C
±1/2 LSB	±1 LSB	PM7528AR	PM7528ER	PM7528GP
±1/2 LSB	±1 LSB	PM7528ARC/883	–	–
±1/2 LSB	±2 LSB	PM7528BR	PM7528FR	–
±1/2 LSB	±2 LSB	PM7528BRC/883	PM7528FP	–
±1/2 LSB	±2 LSB	–	PM7528FPC	–
±1/2 LSB	±2 LSB	–	PM7528FS	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

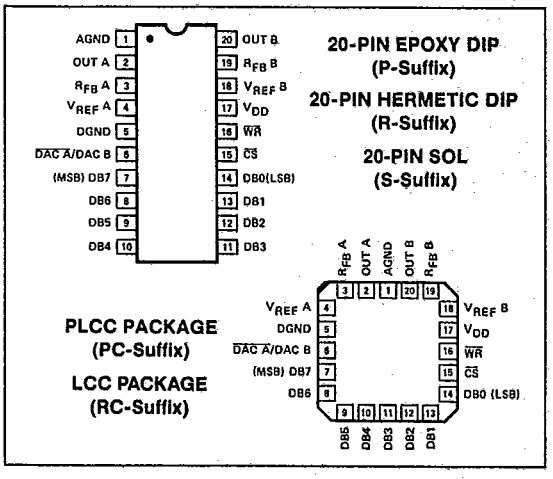
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PM-7528 contains two 8-bit multiplying digital-to-analog converters. Excellent DAC-to-DAC matching and tracking results from monolithic construction. The PM-7528 consists of two thin-film R-2R resistor-ladder networks, tracking span resistors, two data latches, one input buffer, and control logic. Operation from a 5 to 15 volt single power supply dissipates only 20mW of power in a space saving 20-pin 0.3" wide DIP. The PM-7528 features circuitry designed to protect against damage from electrostatic discharges.

Digital input data is directed into one of the DAC data latches determined by the DAC selection control line $\overline{\text{DAC A}}$/DAC B. The 8-bit wide input data path provides TTL/CMOS compatibility. The data load cycle is similar to the write cycle of a random access memory. The PM-7528 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80.

PIN CONNECTIONS



PM-7528

T-51-09-08

ABSOLUTE MAXIMUM RATINGS
(T_A=+25°C, unless otherwise noted)

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... 0V, V_{DD}
Digital Input Voltage to DGND ..... –0.3V, +15V
$V_{PIN\ 2}$, $V_{PIN\ 20}$ to AGND .....–0.3V, +15V
$V_{REF}A$, $V_{REF}B$ to AGND .....±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND .....±25V
Operating Temperature Range
AR, ARC, BR,BRC Versions .....–55°C to ±125°C
ER, FR, FP, FPC, FS Versions .....–40°C to +85°C
GP Version .....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature .....–65°C to +150°C
Lead Temperature (Soldering, 60 sec) .....+300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	80	15	°C/W
20-Pin Plastic DIP (P)	74	32	°C/W
20-Contact LCC (RC)	76	36	°C/W
20-Pin SO (S)	89	27	°C/W
20-Contact PLCC (PC)	98	38	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper antistatic handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A$ = $V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = –55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = –40°C to +85°C apply for PM-7528ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM7528GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM-7528 MIN	PM-7528 TYP	PM-7528 MAX	UNITS
STATIC ACCURACY (Note 1)							
Resolution	N			8	—	—	Bits
Relative Accuracy (Note 2)	NL			—	—	±1/2	LSB
Differential Nonlinearity (Note 3)	DNL			—	—	±1	LSB
Full Scale Gain Error (Note 4)	G_{FSE}	T_A = +25°C	PM7528A/E/G	—	—	±1	LSB
			PM7528B/F	—	—	±2	
		V_{DD} = +5V, T_A = Full Temp. Range	PM7528A/E/G	—	—	±3	
			PM7528B/F	—	—	±4	
		V_{DD} = +15V, T_A = Full Temp. Range	PM7528A/E/G	—	—	±1	
			PM7528B/F	—	—	±3	
Gain Temperature Coefficient (ΔGain/ΔTemperature) (Notes 4, 10)	TCG_{FS}	V_{DD} = +5V		—	—	±0.007	%/°C
		V_{DD} = +15V		—	—	+0.0035	
Output Leakage Current Out A (Pin 2)/Out B (Pin 20) (Note 5)	I_{LKG}	T_A = +25°C		—	5	±50	nA
		V_{DD} = +5V, T_A = Full Temp. Range		—	—	±400	
		V_{DD} = +15V, T_A = Full Temp. Range		—	—	+200	
Input Resistance (V_{REF} A, V_{REF} B) (Note 6)	R_{REF}			8	—	15	kΩ
V_{REF} A/V_{REF} B (Input Resistance Match)	ΔV_{REF} A, B			—	0.1	±1	%

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = −55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = −40°C to +85°C apply for PM-7528ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM7528GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7528 MIN	TYP	MAX	UNITS
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}	V_{DD} = +5V V_{DD} = +15V	2.4 13.5	— —	— —	V
Digital Input Low (Note 8)	V_{INL}	V_{DD} = +5V V_{DD} = +15V	— —	— —	0.8 1.5	V
Input Current (Note 7)	I_{IN}	T_A = +25°C T_A = Full Temp. Range	— —	.001 —	±1 ±10	µA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 $\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$/DAC B	— —	— —	10 15	pF
SWITCHING CHARACTERISTICS at V_{DD} = +5V (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	T_A = +25°C T_A = Full Temp. Range	200 230	— —	— —	ns
Chip Select to Write Hold Time	t_{CH}	T_A = +25°C T_A = Full Temp. Range	20 30	— —	— —	ns
DAC Select to Write Set-Up Time	t_{AS}	T_A = +25°C T_A = Full Temp. Range	200 230	— —	— —	ns
DAC Select to Write Hold Time	t_{AH}	T_A = +25°C T_A = Full Temp. Range	20 30	— —	— —	ns
Data Valid to Write Set-Up Time	t_{DS}	T_A = +25°C T_A = Full Temp. Range	110 130	— —	— —	ns
Data Valid to Write Hold Time	t_{DH}		0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C T_A = Full Temp. Range	180 200	— —	— —	ns
SWITCHING CHARACTERISTICS at V_{DD} = +15V (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	T_A = +25°C T_A = Full Temp. Range	60 80	— —	— —	ns
Chip Select to Write Hold Time	t_{CH}	T_A = +25°C T_A = Full Temp. Range	10 15	— —	— —	ns
DAC Select to Write Set-Up Time	t_{AS}	T_A = +25°C T_A = Full Temp. Range	60 80	— —	— —	ns
DAC Select to Write Hold Time	t_{AH}	T_A = +25°C T_A = Full Temp. Range	10 15	— —	— —	ns
Data Valid to Write Set-Up Time	t_{DS}	T_A = +25°C T_A = Full Temp. Range	50 70	— —	— —	ns
Data Valid to Write Hold Time	t_{DH}		10	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C T_A = Full Temp. Range	60 80	— —	— —	ns

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = −55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = −40°C to +85°C apply for PM-7528ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM7528GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7528 MIN	PM-7528 TYP	PM-7528 MAX	UNITS
POWER SUPPLY (Note 12)						
Supply Current (Note 21)	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	1	mA
		All Digital Inputs 0V or V_{DD}	—	—	100	µA
AC PERFORMANCE CHARACTERISTICS (Note 13)						
DC Supply Rejection Ratio ($\Delta Gain/\Delta V_{DD}$) (Note 14)	PSRR	V_{DD} = +5V				%/%
		T_A = +25°C	—	—	0.02	
		T_A = Full Temp. Range	—	—	0.04	
		V_{DD} = +15V				
		T_A = +25°C	—	—	0.01	
		T_A = Full Temp. Range	—	—	0.02	
Propagation Delay (Notes 15, 16, 17)	t_{pD}	V_{DD} = +5V				ns
		T_A = +25°C	—	—	220	
		T_A = Full Temp. Range	—	—	270	
		V_{DD} = +15V				
		T_A = +25°C	—	—	80	
		T_A = Full Temp. Range	—	—	100	
Current Settling Time (Notes 16, 17, 22)	t_s	V_{DD} = +5V				ns
		T_A = +25°C	—	—	350	
		T_A = Full Temp. Range	—	—	400	
		V_{DD} = +15V				
		T_A = +25°C	—	—	180	
		T_A = Full Temp. Range	—	—	200	
Digital Charge Injection (Note 18)	Q	T_A = +25°C				nVs
		V_{DD} = +5V	—	160	—	
		V_{DD} = +15V	—	440	—	
Output Capacitance	C_{OUT} A	DAC Latches Loaded	—	—	50	pF
	C_{OUT} B	with 00000000	—	—	50	
	C_{OUT} A	DAC Latches Loaded	—	—	120	
	C_{OUT} B	with 11111111	—	—	120	
AC Feedthrough (Note 19)	FT_A	V_{REF} A to OUT A;				dB
		T_A = +25°C	—	—	−70	
		T_A = Full Temp. Range	—	—	−65	
	FT_B	V_{REF} B to OUT B;				
		T_A = +25°C	—	—	−70	
		T_A = Full Temp. Range	—	—	−65	

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A$ = $V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = –55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = –40°C to +85°C apply for PM-7528ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM7528GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7528 MIN	PM-7528 TYP	PM-7528 MAX	UNITS
AC PERFORMANCE CHARACTERISTICS (Note 13)						
Channel-to-Channel Isolation (Note 20)	CCI_{BA}	V_{REF} A to OUT B; V_{REF} A = $20V_{p-p}$ Sinewave @ f = 100kHz V_{REF} B = 0V. T_A = +25°C	—	–77	—	dB
	CCI_{AB}	V_{REF} B to OUT A; V_{REF} B = $20V_{p-p}$ Sinewave @ f = 100kHz V_{REF} A = 0V. T_A = +25°C	—	–77	—	
Digital Crosstalk	Q	For Code Transition From 00000000 to 11111111. T_A = +25°C V_{DD} = +5V	—	30	—	nVs
		V_{DD} = +15V	—	60	—	
Harmonic Distortion	THD	V_{IN} = 6Vrms @ f = 1kHz. T_A = +25°C	—	–85	—	dB

NOTES:

1. Specifications apply to both DAC A and DAC B.
2. This is an endpoint linearity specification.
3. All grades guaranteed to be monotonic over the full operating temperature range.
4. Measured using internal R_{FB} A and R_{FB} B. Both DAC latches loaded with 11111111. Gain error is adjustable using circuits of Figures 5 and 6.
5. DAC loaded with 00000000.
6. Input resistance TC = +50ppm/°C; typical input resistance = 11kΩ.
7. V_{IN} = 0V or V_{DD}.
8. For all data bits DB0-DB7, $\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$/DAC B.
9. Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
10. Guaranteed and not tested.
11. See timing diagram.
12. See Figure 3.
13. These characteristics are for design guidance only and are not subject to test.
14. ΔV_{DD} = ±5%.
15. From digital input to 90% of final analog-output current.
16. V_{REF} A = V_{REF} B = +10V; OUT A, OUT B load = 100Ω, C_{EXT} = 13pF.
17. $\overline{WR}$, $\overline{CS}$ = 0V, DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
18. For code transition 00000000 to 11111111.
19. V_{REF} A, V_{REF} B = $20V_{p-p}$ Sinewave @ f = 100kHz.
20. Both DAC latches loaded with 11111111.
21. I_{DD} = 500μA at T_A = Full Temp. Range.
22. Extrapolated: t_s (1/2 LSB) = t_pD + 6.2τ, where τ = the measured first time constant of the final RC decay.

PM-7528

DICE CHARACTERISTICS

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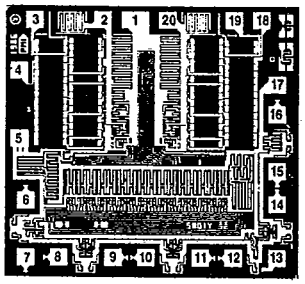

DIE SIZE 0.086 × 0.092 inch, 7,192 sq. mils
(2.184 × 2.337 mm, 5.105 sq. mm)

1. ANALOG GROUND (AGND)
2. OUTPUT A (OUT A)
3. DAC A FEEDBACK RESISTOR ($R_{FB}A$)
4. DAC A REFERENCE INPUT ($V_{REF}A$)
5. DIGITAL GROUND (DGND)
6. DIGITAL SELECTION ($\overline{DAC}$ A/DAC B)
7. DIGITAL INPUT DB7 (MSB)
8. DIGITAL INPUT DB6
9. DIGITAL INPUT DB5
10. DIGITAL INPUT DB4
11. DIGITAL INPUT DB3
12. DIGITAL INPUT DB2
13. DIGITAL INPUT DB1
14. DIGITAL INPUT DB0 (LSB)
15. CHIP SELECT ($\overline{CS}$)
16. WRITE ($\overline{WR}$)
17. POSITIVE POWER SUPPLY (V_{DD})
18. DAC B REFERENCE INPUT ($V_{REF}B$)
19. DAC B FEEDBACK RESISTOR ($R_{FB}B$)
20. OUTPUT B (OUT B)

WAFER TEST LIMITS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7528G LIMIT	UNITS
Relative Accuracy	NL	Endpoint Linearity Error	±½	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 11111111	±2	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 00000000 Pad 2 and 20	±50	nA MAX
Input Resistance	R_{REF}	Pad 4 and 18	8/15	KΩMIN/ KΩMAX
$V_{REF}A/V_{REF}B$ Input Resistance Match	$\Delta V_{REF}A, B$		±1	% MAX
Digital Input High	V_{IH}	V_{DD} = 5V V_{DD} = 15V	2.4 13.5	V_{MIN}
Digital Input Low	V_{IL}	V_{DD} = 5V V_{DD} = 15V	0.8 1.5	V_{MAX}
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	1 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV_{DD})	PSRR	V_{DD} = ±5%	0.02	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, $V_{REF}A = V_{REF}B$ = +10V, OUT A = OUT B = 0V; T_A = 25°C, unless otherwise noted. (Note 13)

PARAMETER	SYMBOL	CONDITIONS	PM-7528G TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		6	pF
Output Capacitance	$C_{OUT}A$ $C_{OUT}B$	DAC Latches Loaded with 00000000	22 22	pF
	$C_{OUT}A$ $C_{OUT}B$	DAC Latches Loaded with 11111111	40 40	pF
Propagation Delay (Notes 15, 16, 17)	t_{pD}	V_{DD} = 15V V_{DD} = 5V	70 150	ns

TYPICAL PERFORMANCE CHARACTERISTICS

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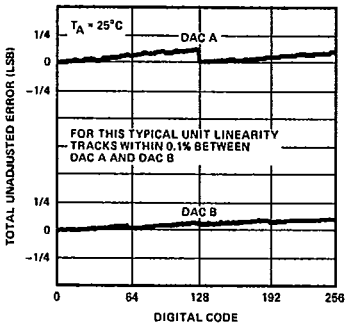
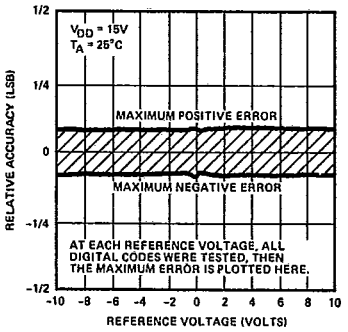
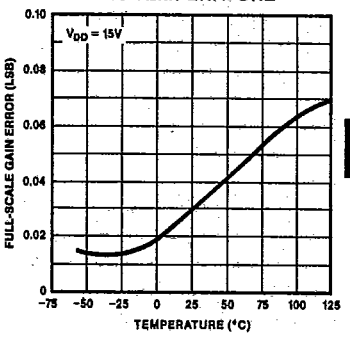
TOTAL UNADJUSTED ERROR vs DIGITAL INPUT



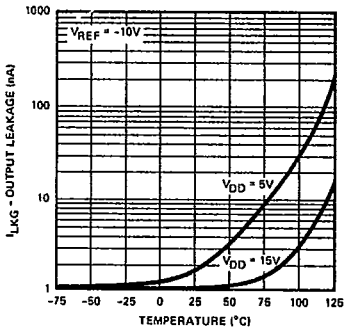
RELATIVE ACCURACY vs REFERENCE VOLTAGE



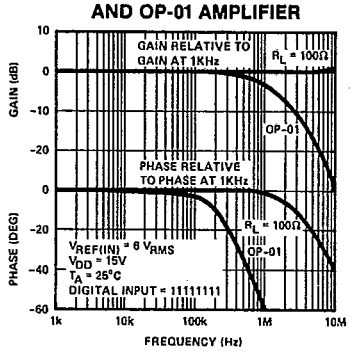
FULL-SCALE GAIN ERROR vs TEMPERATURE



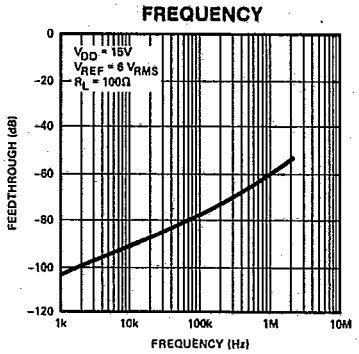
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



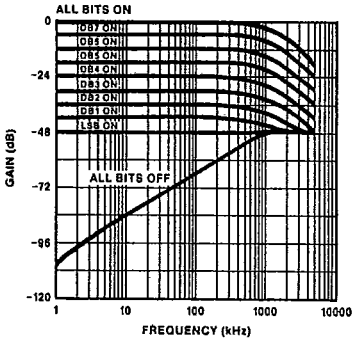
GAIN AND PHASE SHIFT vs FREQUENCY WITH RESISTIVE LOAD AND OP-01 AMPLIFIER



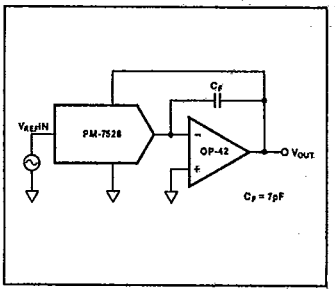
FEEDTHROUGH vs FREQUENCY



GAIN ($V_{OUT}/V_{REF}IN$) vs FREQUENCY

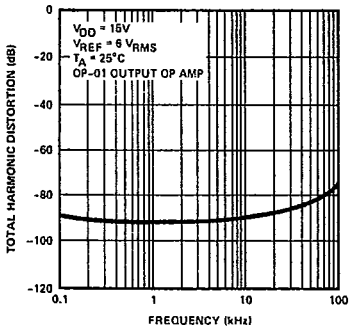


TEST CIRCUIT FOR GAIN vs FREQUENCY

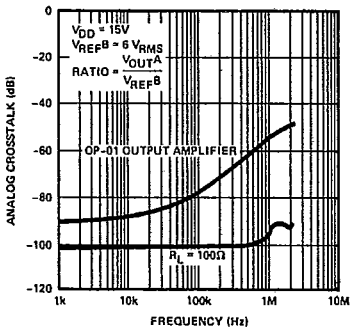


TYPICAL PERFORMANCE CHARACTERISTICS

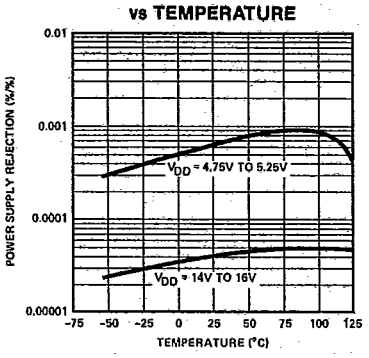
TOTAL HARMONIC DISTORTION vs FREQUENCY



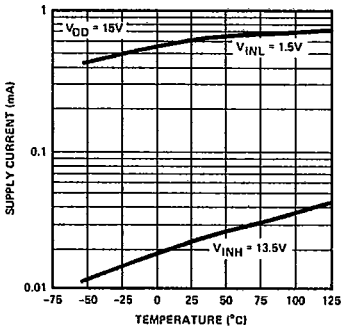
ANALOG CROSSTALK vs FREQUENCY



POWER SUPPLY REJECTION vs TEMPERATURE

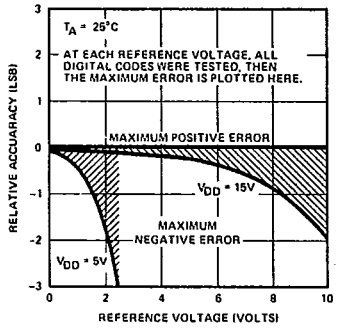


SUPPLY CURRENT vs TEMPERATURE

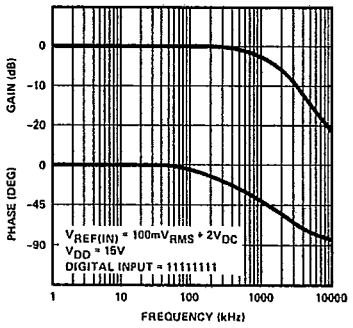


VOLTAGE SWITCHING MODE CHARACTERISTICS

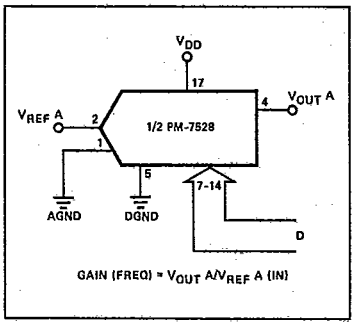
RELATIVE ACCURACY vs REFERENCE VOLTAGE



GAIN AND PHASE vs FREQUENCY



VOLTAGE SWITCHING MODE TEST CIRCUIT



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Relative accuracy, or endpoint nonlinearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale, and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error, or full-scale error, is a measure of the output error between an ideal DAC and the actual device output. The ideal full-scale output is V_{REF} minus 1 LSB. Gain error of both DAC's in the PM-7528 is adjustable to zero with external resistance.

OUTPUT CAPACITANCE

Capacitance from OUT A or OUT B to AGND.

DIGITAL CHARGE INJECTION

The amount of charge injected from the digital inputs to the analog output when the inputs change states. This is normally specified as the area of the glitch in either pAsecs or nVsecs, depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REF} A, V_{REF} B = AGND.

PROPAGATION DELAY

This is a measure of the internal delays of the circuit. It is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

CHANNEL-TO-CHANNEL ISOLATION

The portion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

DIGITAL CROSSTALK

The glitch energy transferred to the output of one converter, due to a change in digital input code to the other converter, specified in nVsec.

AC FEEDTHROUGH

AC signal due to capacitive coupling from V_{REF} to output with all switches "off."

INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

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MODE SELECTION

The inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0–DB7.

HOLD MODE

The selected DAC latch retains the data which was present on the data lines just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

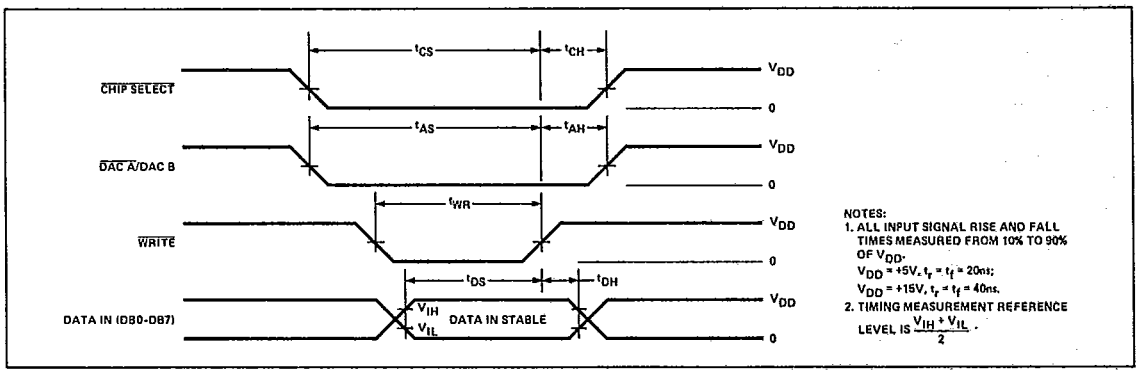
$\overline{\text{DAC A}}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

CIRCUIT INFORMATION—D/A SECTION

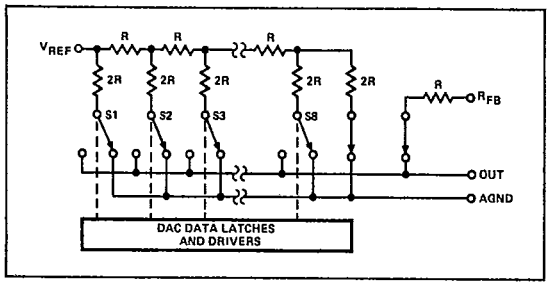
The PM-7528 contains two identical 8-bit multiplying digital-to-analog converters, DAC A and DAC B. Each DAC includes a stable thin-film R-2R resistor ladder and eight NMOS current steering switches. Figure 1 shows a simplified equivalent circuit

WRITE CYCLE TIMING DIAGRAM



of either DAC. The inverted R-2R ladder takes a voltage or current reference and divides it in a binary manner among the eight current steering switches. The number of switches selected to the output (OUT) add their currents together forming an analog output current representation of the switch selection. The DAC OUT and analog ground (AGND) should be maintained at the same voltage for proper operation. The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves linearity performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

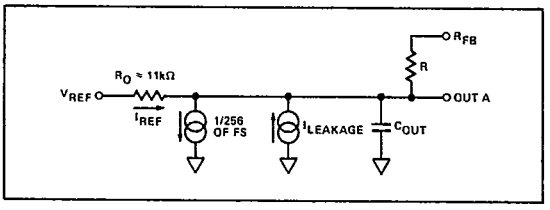
FIGURE 1: Simplified functional circuit for DAC A or DAC B.



EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit of DAC A shown in Figure 2 is similar to DAC B. DAC A and DAC B both share the analog ground pin 1 (AGND). With all digital inputs high, the reference current flows to OUT A. A small leakage current ($I_{LEAKAGE}$) flows across internal junctions, doubling every 10°C. The R-2R ladder termination resistor generates a constant 1/256 current which is 1 LSB of the reference current (I_{REF}). C_{OUT} is the parallel combination of the NMOS current steering switches. The value of C_{OUT} depends on the number of switches connected to the output. The range of C_{OUT} is 50pF to 120pF maximum. The equivalent output resistance R_O varies with input code from 0.8R to 3R, where R is the nominal ladder resistor of the R-2R ladder.

FIGURE 2: PM-7528 DAC A equivalent circuit. All digital inputs high.

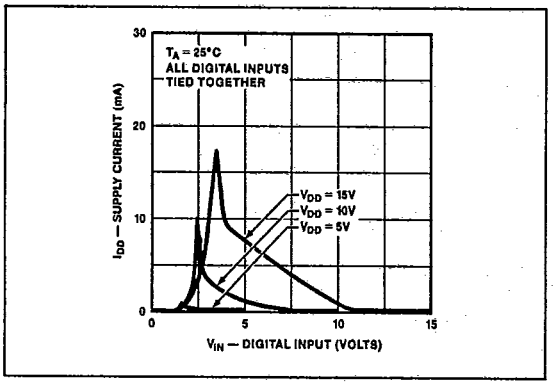


CIRCUIT INFORMATION—DIGITAL SECTION

The digital inputs provide TTL input compatibility (V_{INH} = 2.4, V_{INL} = 0.8V) when the PM-7528 operates with V_{DD} of +5V. The digital inputs effect the amount of quiescent supply current as shown in Figure 3. Peak supply current occurs as the digital input (V_{IN}) passes through the transition voltage. Maintaining the digital input voltages as close as possible to the supplies (V_{DD} and DGND) minimizes supply current consumption. When operating the PM-7528 from CMOS logic the digital inputs are driven very close to the supply rails, minimizing power consumption.

Digital input protection from electrostatic discharge and electrostatic buildup occurs in the input network shown in Figure 4.

FIGURE 3: Typical plots of supply current, I_{DD} vs logic input voltage (V_{IN}), for V_{DD} = +5V, +10V, and +15V.



BURN-IN CIRCUIT

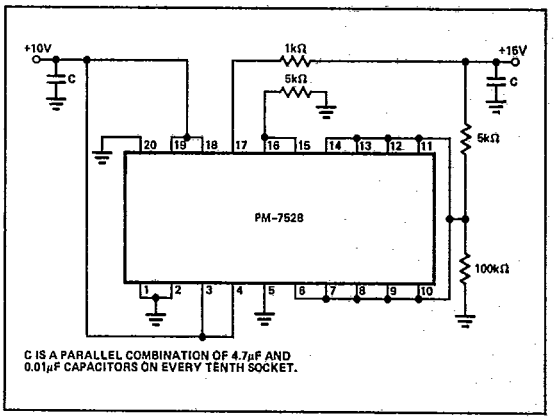
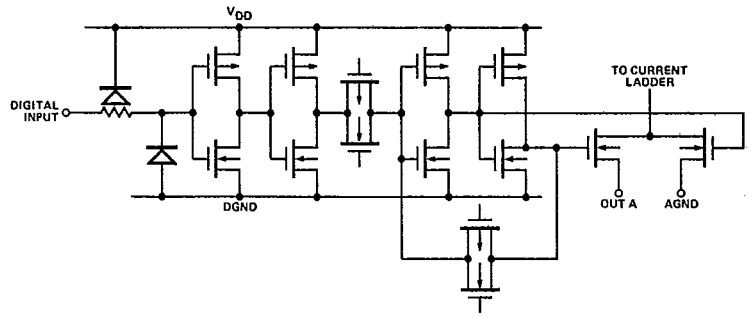


FIGURE 4: Simplified equivalent gate-input protection circuit. One of eight current switches, and its associated internal CMOS-drive-circuitry, is shown.



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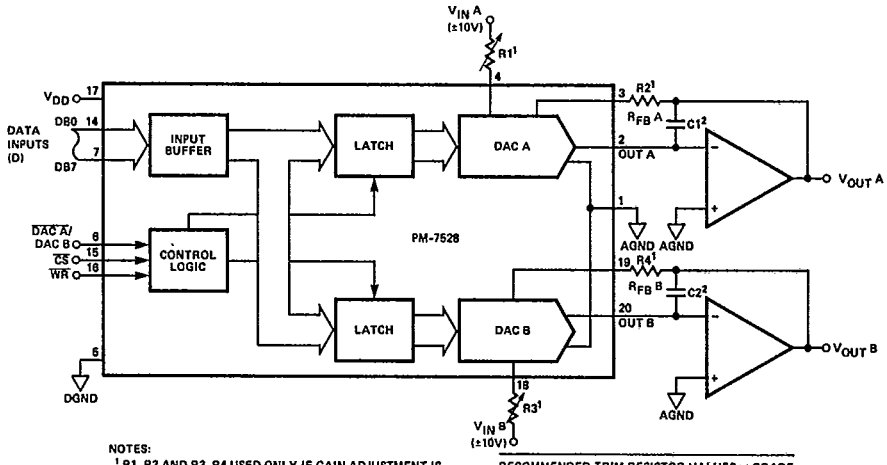
APPLICATIONS INFORMATION

The most common application of this DAC is voltage output operation. Unipolar output operation provides a 0 to 10 volt output swing when connected, as shown in Figure 5. The maximum output voltage polarity is the inverse of the input reference voltage, since the op amp inverts the input currents. The transfer equation for unipolar operation is $V_{OUT} = -V_{IN} \times D/256$, where D is the decimal value of the data bit inputs DB0 thru DB7 and V_{IN} is the reference input voltage. The transfer equation highlights another popular application of CMOS DAC's, multiplication. The output voltage is the product of the reference voltage and the digital input code. The reference input voltage can be any value in the range of ±25 volts for both DC or AC signals. The circuit in Figure 5 performs two-quadrant multiplication. Table 1 provides example analog outputs for the given digital input codes.

For bipolar output operation connect the PM-7528 as shown in Figure 6. This circuit configuration provides an offset current, derived from the reference, to enable the output op amp to swing in both polarities. The digital input coding becomes offset binary. Table 2 provides some example analog outputs for various digital inputs (D). The transfer equation for bipolar operation is $V_{OUT} = V_{IN} \times (D/128 - 1)$, where D is the decimal value of the data bit inputs DB0 thru DB7. This circuit provides full four-quadrant multiplication able to accept both polarities on all inputs as well as the circuit output.

FIGURE 5: Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.



NOTES:
[1] R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE FOR RECOMMENDED VALUES. MAKE GAIN ADJUSTMENT WITH DIGITAL INPUT OF 255.
[2] C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

RECOMMENDED TRIM RESISTOR VALUES vs GRADE

TRIM RESISTOR	HP/FR/BR	GP/ER/AR
R1, R3	500Ω	200Ω
R2, R4	150Ω	82Ω

TABLE 1: Unipolar Binary Code Table. See Figure 5.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
11111111	$-V_{IN}\left(\frac{255}{256}\right)$
10000001	$-V_{IN}\left(\frac{129}{256}\right)$
10000000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
01111111	$-V_{IN}\left(\frac{127}{256}\right)$
00000001	$-V_{IN}\left(\frac{1}{256}\right)$
00000000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

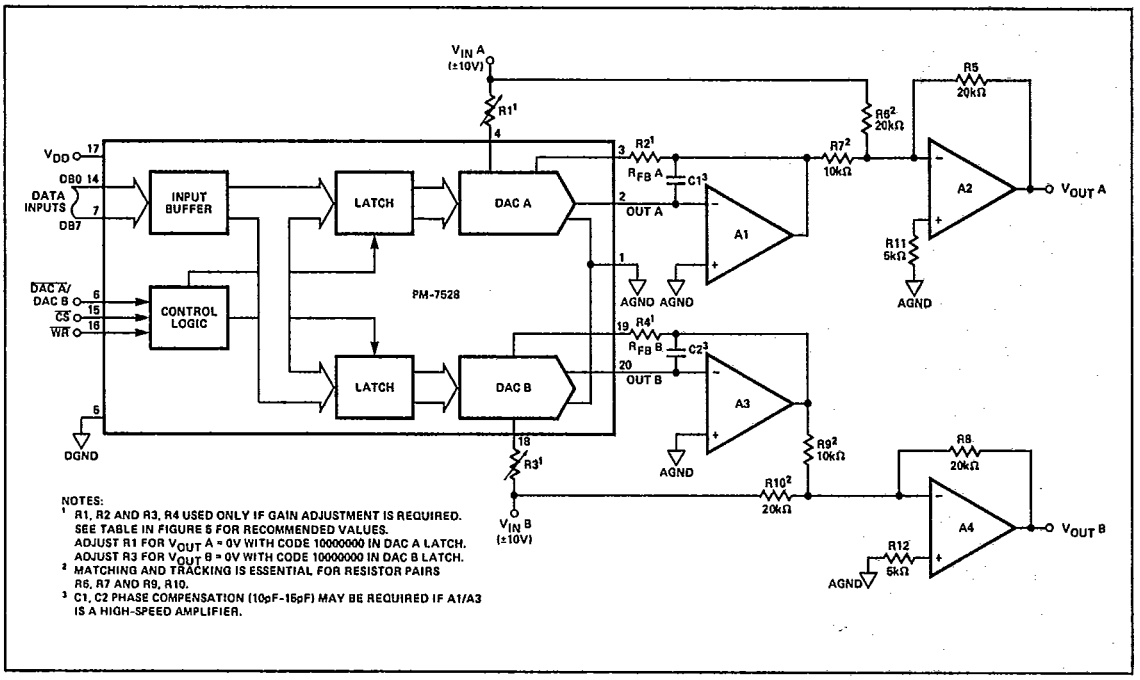
NOTE: 1 LSB = $(2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

TABLE 2: Bipolar (Offset Binary) Code Table. See Figure 6.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT (DAC A or DAC B)
11111111	$+V_{IN}\left(\frac{127}{128}\right)$
10000001	$+V_{IN}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{IN}\left(\frac{1}{128}\right)$
00000001	$-V_{IN}\left(\frac{127}{128}\right)$
00000000	$-V_{IN}\left(\frac{128}{128}\right)$

NOTE: 1 LSB = $(2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

FIGURE 6: Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.



APPLICATION HINTS

To ensure system performance consistent with PM-7528 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the PM-7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal, is to tie AGND and DGND together at the PM-7528. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes (1N914 or equivalent) be connected in inverse parallel between the PM-7528 AGND and DGND pins.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output with a maximum magnitude of 0.67 V_{OS} (V_{OS} is amplifier input-offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
3. HIGH-FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open-loop response; this can cause ringing or oscillation. Stability can be restored by adding a phase-compensation capacitor in parallel with the feedback resistor.
4. DYNAMIC PERFORMANCE: The dynamic performance of the two DACs in the PM-7528 will depend upon the gain and phase characteristics of the output amplifiers, together with the optimum choice of the PC board layout and decoupling components.
5. CIRCUIT LAYOUT SUGGESTIONS: Analog and digital ground traces should be routed between package pins to isolate the digital inputs from the analog circuitry. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, 4-5 to minimize reference feedthrough to the output in multiplying applications. A power supply bypass capacitor (0.1μF) is recommended across V_{DD} to DGND.

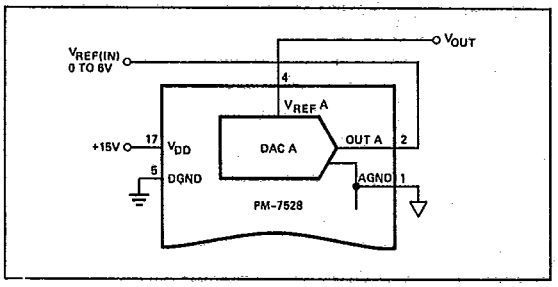
SINGLE SUPPLY OPERATION, VOLTAGE SWITCHING

With the PM-7528 connected in the voltage switching mode of operation, Figure 7, only one power supply is necessary. There is no voltage inversion between the reference input polarity and the output in the voltage switching mode.

Two characteristic curves in the typical performance characteristics section were generated using this voltage switching mode of operation. The first graph, linearity error versus input reference voltage, shows that to maintain a ±1/2 LSB maximum linearity error, V_{REF} should be less than 1.5 volts for V_{DD} = 5 volts or less than 6 volts for V_{DD} = 15 volts. The gain-phase response graph shows a dominant pole response for single supply applications where the reference input is an AC signal. In this application the reference input should remain between 1.5 volts and ground when V_{DD} = 5 volts. Additionally settling time measures 400 to 500 nano seconds for a digital input change of 255 to 0 when V_{DD} = 5V.

The output terminal in the voltage switching mode has a constant output resistance (≈ 11K Ω) independent of the digital input code. The output should be buffered with a voltage follower when driving low impedance loads.

FIGURE 7: PM-7528 in Single Supply, Voltage Switching Mode



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SINGLE SUPPLY, CURRENT SWITCHING

An alternate single-supply operating mode of the PM-7528 results when offsetting the analog ground. Figure 8 shows the method of connection. The advantage of this connection method is the ability to set the output voltage swing in the center of the supply voltage. This allows use of lower cost op amps that would not work in single-supply voltage-switching applications.

The transfer equation in this mode of operation is;

$V_{OUT}(D) = D/256\ (AGND - V_{REF}) + AGND$

where D is the whole number binary input

A popular connection in the current-steering single-supply mode consists of a 2.5 volt reference connected to AGND, the V_{REF} input grounded, V_{DD} connected to 5 volts and the external (V+) op amp tied to 12 volts. This hookup results in the following transfer equation;

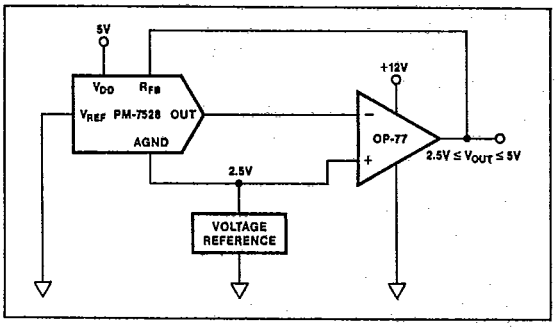
$V_{OUT}(D) = 2.5\ (1 + D/256)$

where $V_{OUT}\ (255) = 2.5\ (1 + 255/256) = 5V$

$V_{OUT}\ (0) = 2.5V$

To maintain best linearity keep AGND equal to or less than 2.5 volts when V_{DD} is 5 volts.

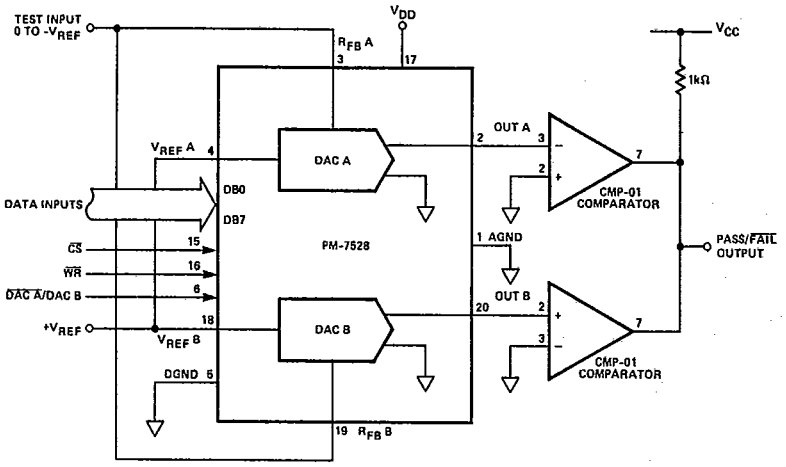
FIGURE 8: PM-7528 in Single Supply, Current-Steering Mode



PROGRAMMABLE WINDOW COMPARATOR

A programmable window-comparator in Figure 9 will determine if voltage inputs applied to the DAC feedback resistors are within limits programmed into the PM-7528 data latches. The input signal range depends on the reference and polarity, that is the test input range is 0 to minus V_{REF}. The A and B data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output to logic high.

FIGURE 9: Digitally Programmable Window Comparator (Upper and Lower Limit Detector).



MICROPROCESSOR INTERFACE

FIGURE 10: PM-7528 Dual DAC to 6800 CPU Interface.

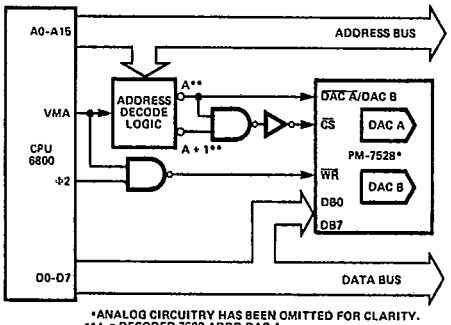
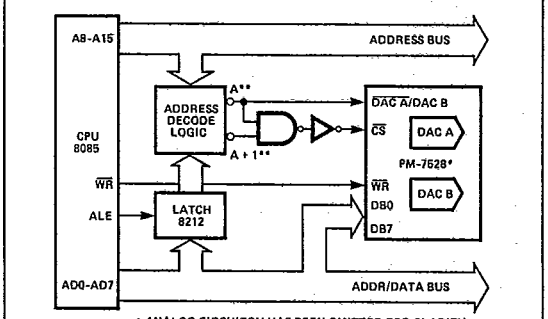


FIGURE 11: PM-7528 Dual DAC to 8085 CPU Interface.



DIGITALLY CONTROLLED SIGNAL ATTENUATOR

Figure 12 shows the PM-7528 configured as a two-channel programmable attenuator. Applications include stereo, audio, and telephone signal-level control applications. In order to generate logarithmic attenuation, Table 4 was generated based on the equation:

$$\text{Digital Input} = 256 \times \exp\left(\frac{-\text{Attenuation (dB)}}{20}\right)$$

FIGURE 12: Digitally-Controlled Dual Telephone Attenuator.

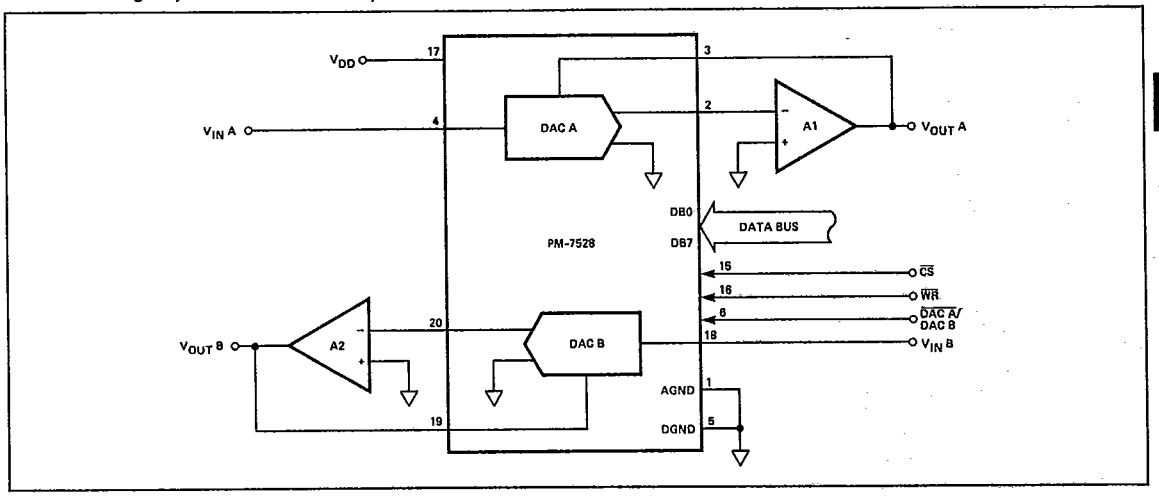


TABLE 4: Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 12

ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL	ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43