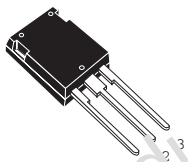
STY100NS20FD

N-channel 200V - 0.022Ω - 100A - Max247
MESH OVERLAY™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STY100NS20FD	200V	<0.024Ω	100A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- ± 20V gate to source voltage rating
- Low intrinsic capacitance
- Fast body-drain diode:low t_{rr}, Q_{rr}

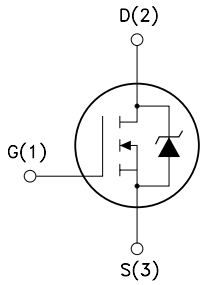


Max247

Description

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The new patented STrip layout coupled with the Company's proprietary edge termination structure, gives the lowest $R_{DS(ON)}$ per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STY100NS20FD	Y100NS20FD	Max247	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source voltage	±20	V
I_D	Drain current (continuos) at T_C = 25°C	100	A
I_D	Drain current (continuos) at T_C = 100°C	63	A
I_{DM} (1)	Drain current (pulsed)	400	A
P_{TOT}	Total dissipation at T_C = 25°C	450	W
	Derating factor	3.6	W/°C
dv/dt (2)	Peak diode recovery voltage slope	25	V/ns
T_{stg}	Storage temperature	–65 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 100A$, di/dt ≤ 200A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case Max	0.277	°C/W
Rthj-amb	Thermal resistance junction-ambient Max	30	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	110	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	750	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, @125°C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 50A		0.022	0.024	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 50A		30		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		7900 1500 460		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 100V, I_D = 100A, V_{GS} = 10V (see Figure 13)		360 35 135		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 100V, I_D = 50A R_G = 4.7Ω V_{GS} = 10V (see Figure 12)		42 140		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 100V, I_D = 100A, R_G = 4.7Ω, V_{GS} = 10V (see Figure 12)		245 140 220		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test condictions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				100	A
I_{SDM} (1)	Source-drain current (pulsed)				400	A
V_{SD} (2)	Forward on voltage	I_{SD} = 100A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=100A, Tj=150°C di/dt = 100A/µs V_{DD}=160V, (see Figure 17)		225 1.35 12		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

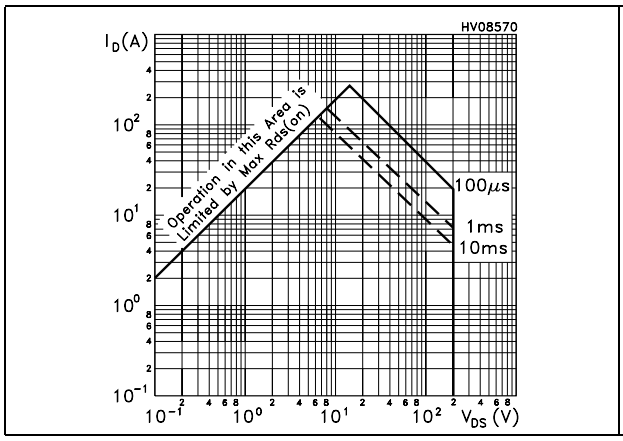


Figure 2. Thermal impedance

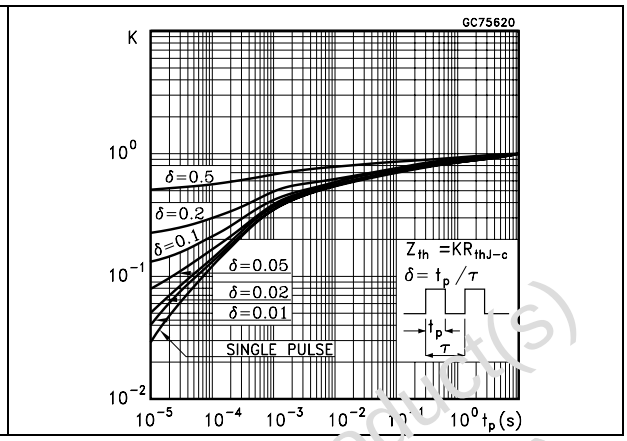


Figure 3. Output characterisics

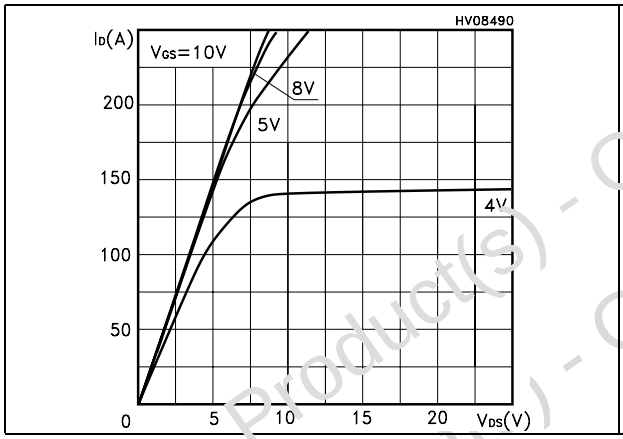


Figure 4. Transfer characteristics

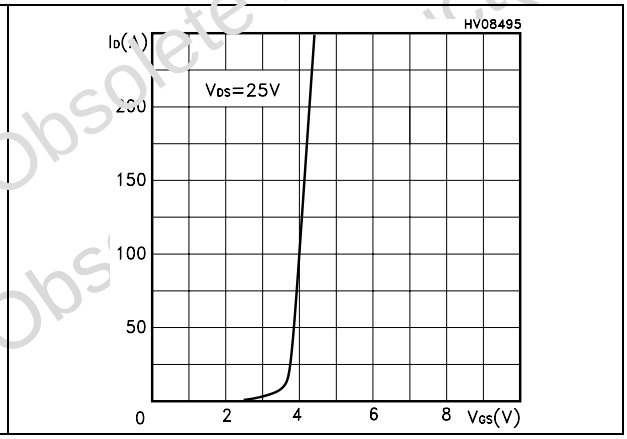


Figure 5. Transconductance

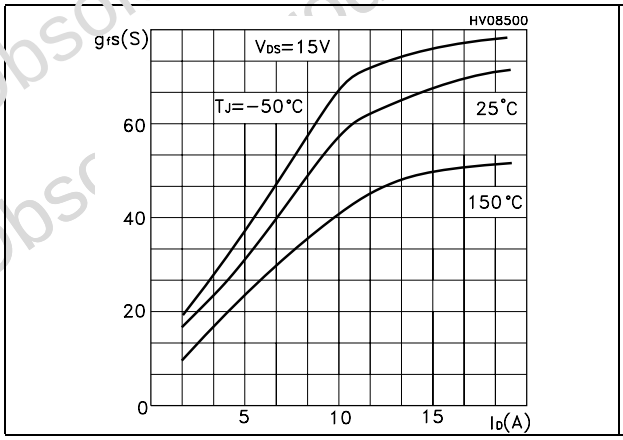


Figure 6. Static drain-source on resistance

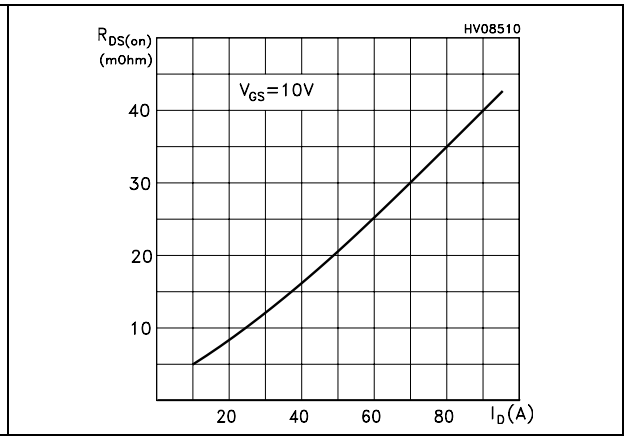


Figure 7. Gate charge vs gate-source voltage

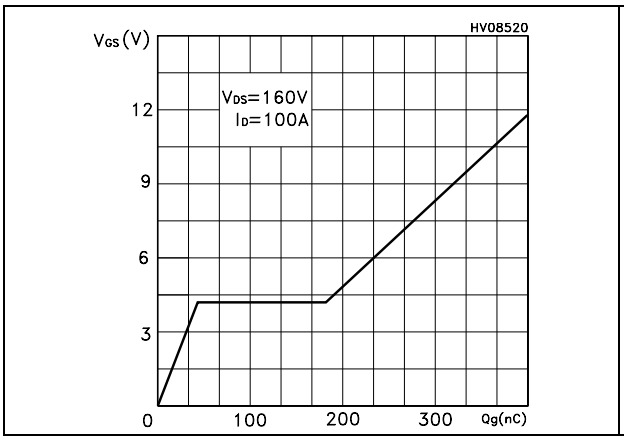


Figure 8. Capacitance variations

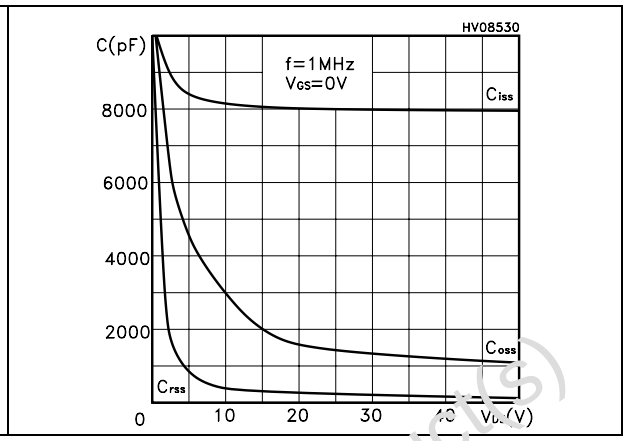


Figure 9. Normalized gate threshold voltage vs temperature

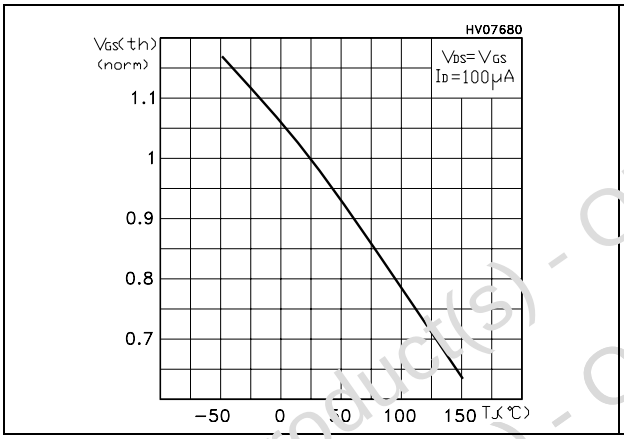


Figure 10. Normalized on resistance vs temperature

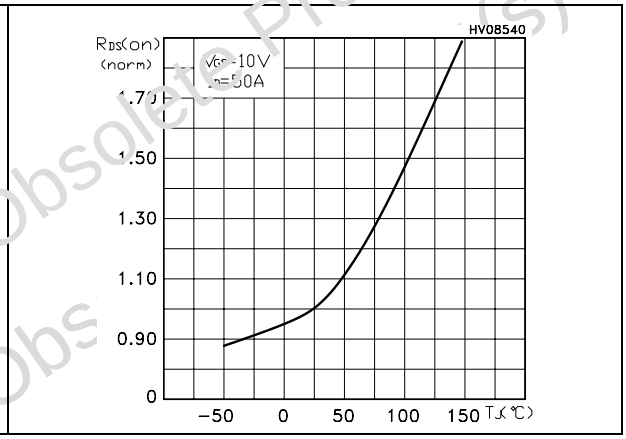
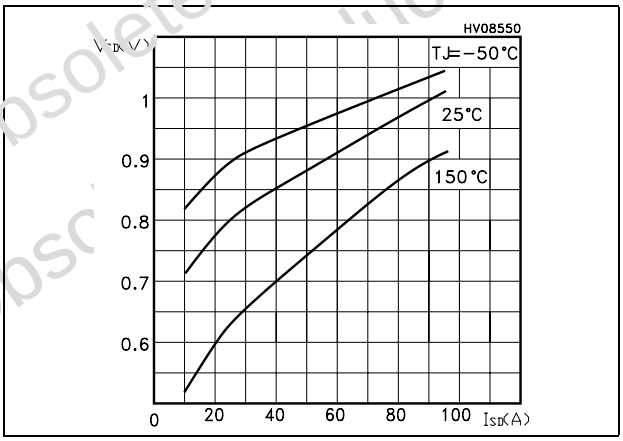


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

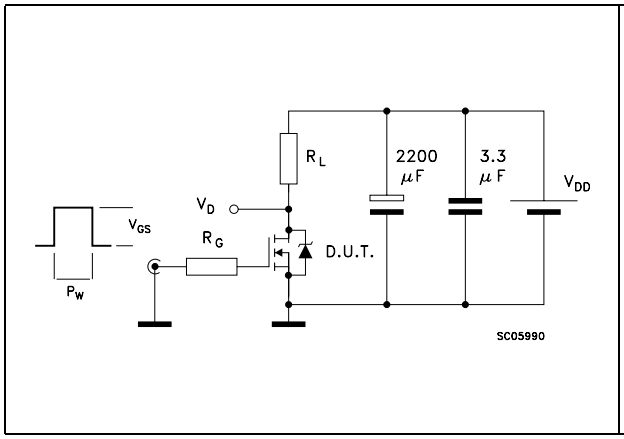


Figure 13. Gate charge test circuit

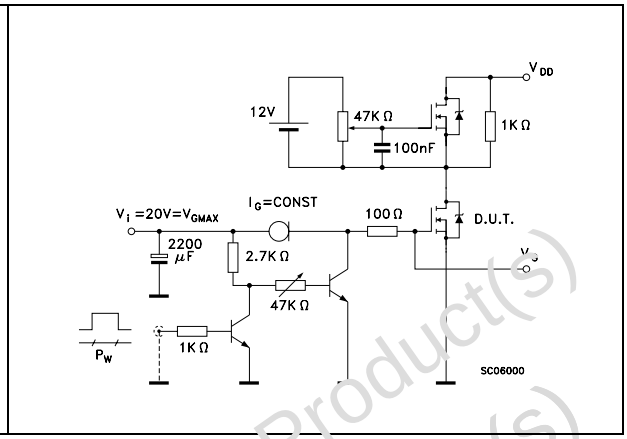


Figure 14. Test circuit for inductive load switching and diode recovery times

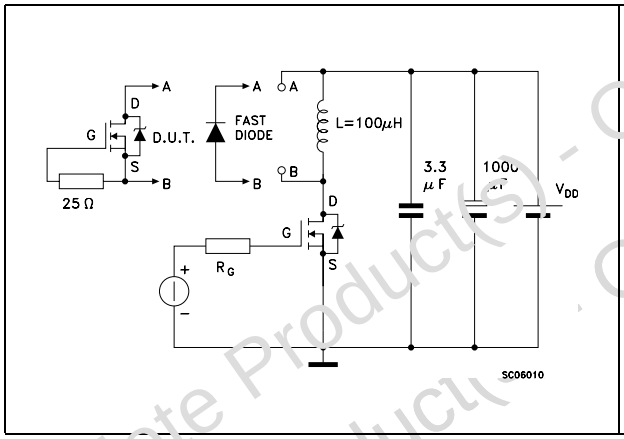


Figure 15. Unclamped inductive load test circuit

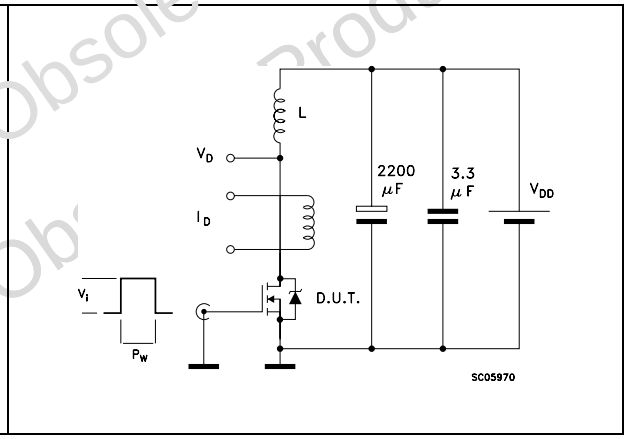


Figure 16. Unclamped inductive waveform

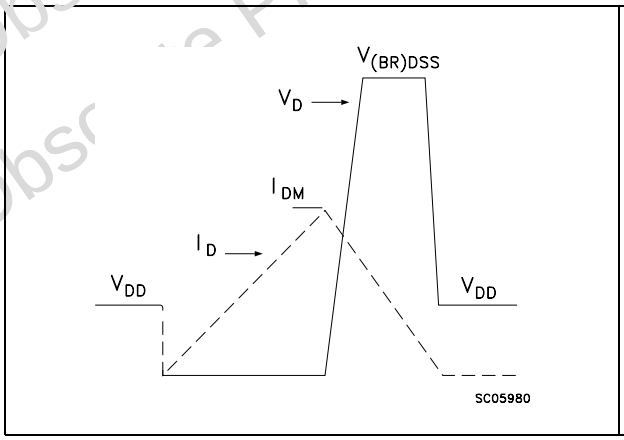
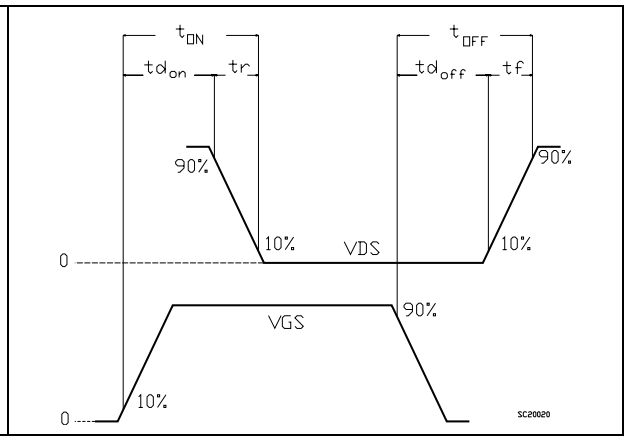


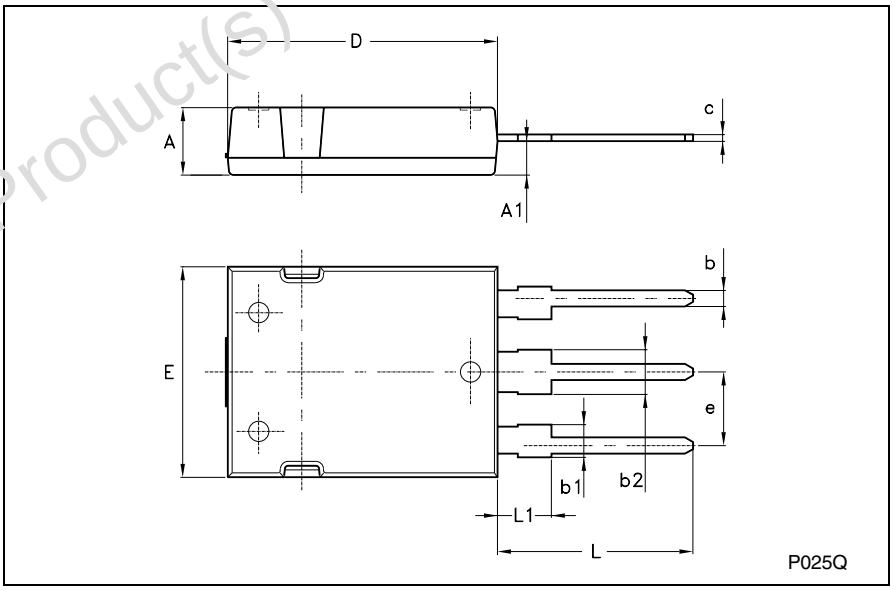
Figure 17. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

Max247 MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



5 Revision history

Table 8. Revision history

Date	Revision	Changes
15-May-2006	3	New template

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