0.8% Accurate Quad Voltage Monitor

ADM1184

FEATURES

- Powered from 2.7 V to 5.5 V on the VCC pin
- Monitors 4 supplies via 0.8% accurate comparators
- 4 inputs can be programmed to monitor different voltage levels with external resistor dividers
- 3 open-drain enable outputs (OUT1, OUT2, and OUT3)
- Open-drain power-good output (PWRGD)
- Internal 190 ms delay associated with assertion of PWRGD
- 10-lead MSOP

APPLICATIONS

- Monitor and alarm functions
- Telecommunications
- Microprocessor systems
- PC/servers

FUNCTIONAL BLOCK DIAGRAM

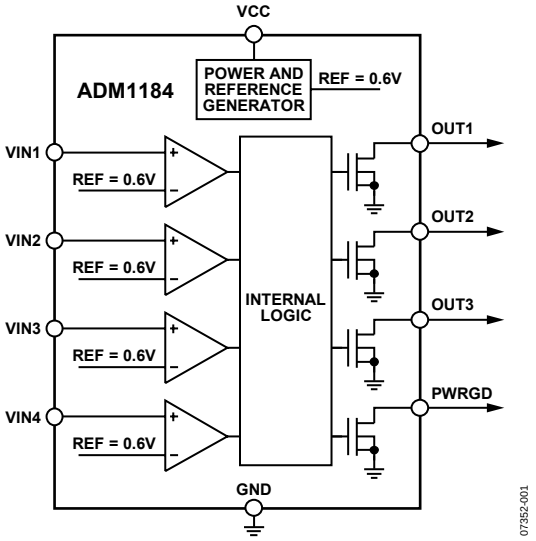

Figure 1.

GENERAL DESCRIPTION

The ADM1184 is an integrated, 4-channel voltage-monitoring device. A 2.7 V to 5.5 V power supply is required on the VCC pin to power the device.

Four precision comparators monitor four voltage rails. Each comparator has a 0.6 V reference with a worst-case accuracy of 0.8%. Resistor networks that are external to the VIN1, VIN2, VIN3, and VIN4 pins set the trip points for the monitored supply rails.

The ADM1184 has four open-drain outputs. OUT1 to OUT3 can be used to enable power supplies, and PWRGD is a common power-good output.

OUT1 to OUT3 are dependent on their associated VINx input (that is, VIN1, VIN2, or VIN3). If a supply monitored by VINx drops below its programmed threshold, the associated OUTx pin and PWRGD are disabled.

PWRGD is a common power-good output indicating the status of all monitored supplies. There is an internal 190 ms (typical) delay associated with the assertion of the PWRGD output. If VIN1, VIN2, VIN3, or VIN4 drops below its programmed threshold, PWRGD is deasserted immediately.

The ADM1184 is available in a 10-lead mini small outline package (MSOP).

Rev. 0

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ADM1184* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADM1184 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1311: Complex Power Supply Sequencing Made Easy

Data Sheet

- ADM1184: 0.8% Accurate Quad Voltage Monitor Data Sheet

REFERENCE MATERIALS

Product Selection Guide

- Supervisory Devices Complementary Parts Guide for Altera FPGAs
- Supervisory Devices Complementary Parts Guide for Xilinx FPGAs

DESIGN RESOURCES

- ADM1184 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADM1184 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

2/08—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2.7 V to 5.5 V, T_A = −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions
VCC Pin					
Operating Voltage Range, V_{CC}	2.7	3.3	5.5	V	
Supply Current, I_{VCC}		24	80	µA	
VIN1 to VIN4 (VINx) Pins					
Input Current, $I_{VINLEAK}$	−20		+20	nA	V_{VINx} = 0.7 V
Input Threshold, V_{TH}	0.5952	0.6000	0.6048	V	
OUT1 to OUT3 (OUTx), PWRGD Pins					
Output Low Voltage, V_{OUTL}			0.4	V	V_{CC} = 2.7 V, I_{SINK} = 2 mA
			0.4	V	V_{CC} = 1 V, I_{SINK} = 100 µA
Leakage Current, I_{ALERT}	−1		+1	µA	
V_{CC} that Guarantees Valid Outputs	1			V	All outputs are guaranteed to be either low or to give a valid output level from V_{CC} = 1 V
TIMING DELAYS					Refer to the timing diagrams in Figure 18 and Figure 19
VIN1 to OUT1, VIN2 to OUT2, VIN3 to OUT3					
Low-to-High Propagation Delay		30		µs	V_{CC} = 3.3 V
High-to-Low Propagation Delay, All Inputs		30		µs	V_{CC} = 3.3 V
All Inputs High to PWRGD Rising Delay	100	190	280	ms	V_{CC} = 3.3 V

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
VCC Pin	−0.3 V to +6 V
VINx Pins	−0.3 V to +6 V
OUTx, PWRGD Pins	−0.3 V to +6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Soldering (10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
10-Lead MSOP	137.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

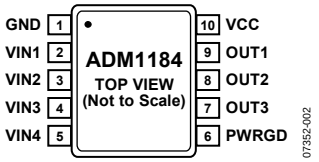


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Chip Ground Pin.
2	VIN1	Noninverting Input of Comparator 1. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider.
3	VIN2	Noninverting Input of Comparator 2. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider.
4	VIN3	Noninverting Input of Comparator 3. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider.
5	VIN4	Noninverting Input of Comparator 4. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider.
6	PWRGD	Active High, Open-Drain Output. When the voltage on each VINx input exceeds 0.6 V, PWRGD is asserted after a 190 ms delay. Once PWRGD has been asserted, if the voltage monitored by VIN1, VIN2, VIN3, or VIN4 falls below 0.6 V, the PWRGD output is deasserted immediately.
7	OUT3	Active High, Open-Drain Output. When the voltage on VIN3 exceeds 0.6 V, OUT3 is asserted. OUT3 remains asserted until the voltage monitored by VIN3 falls below 0.6 V, and then it is driven low.
8	OUT2	Active High, Open-Drain Output. When the voltage on VIN2 exceeds 0.6 V, OUT2 is asserted. OUT2 remains asserted until the voltage monitored by VIN2 falls below 0.6 V, and then it is driven low.
9	OUT1	Active High, Open-Drain Output. When the voltage on VIN1 exceeds 0.6 V, OUT1 is asserted. OUT1 remains asserted until the voltage monitored by VIN1 falls below 0.6 V, and then it is driven low.
10	VCC	Positive Supply Input Pin. The operating supply voltage range is 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

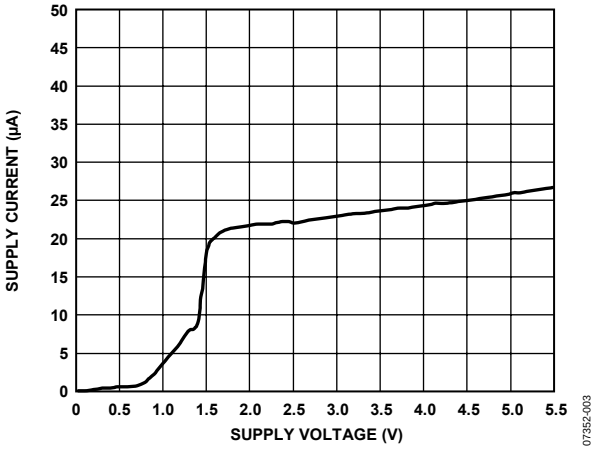


Figure 3. Supply Current vs. Supply Voltage

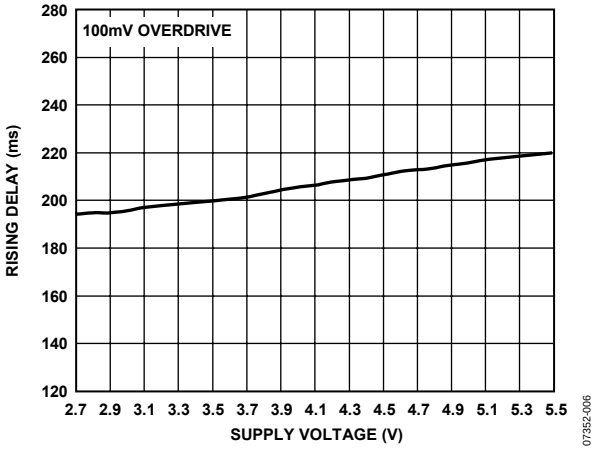


Figure 6. All Inputs High to PWRGD Rising Delay vs. Supply Voltage

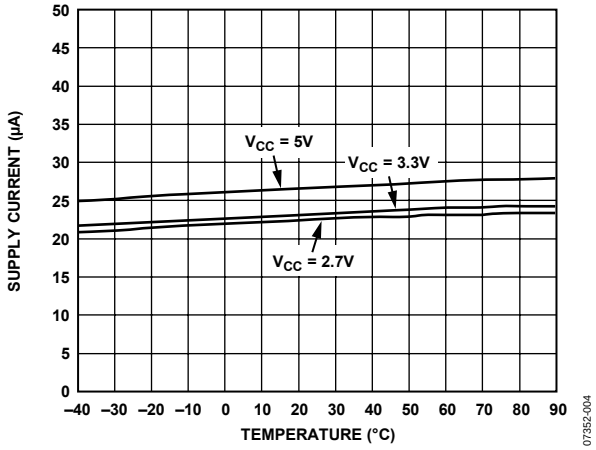


Figure 4. Supply Current vs. Temperature

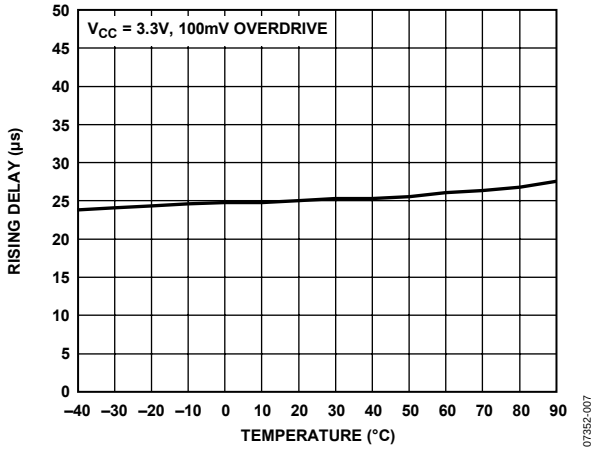


Figure 7. VIN1/VIN2/VIN3 to OUT1/OUT2/OUT3 Rising Delay vs. Temperature

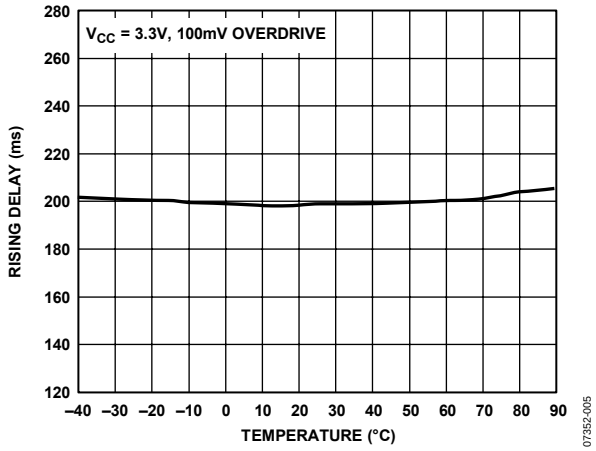


Figure 5. All Inputs High to PWRGD Rising Delay vs. Temperature

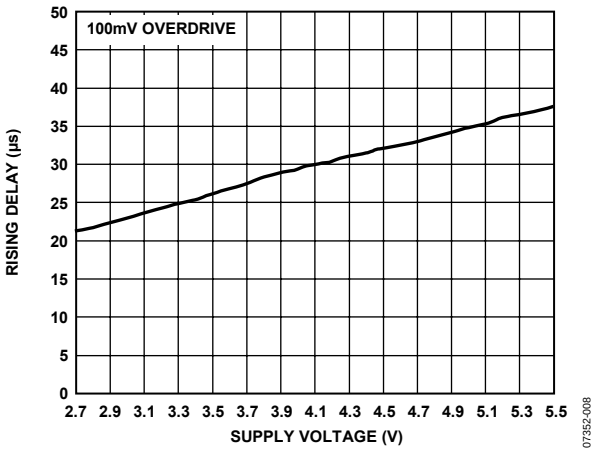


Figure 8. VIN1/VIN2/VIN3 to OUT1/OUT2/OUT3 Rising Delay vs. Supply Voltage

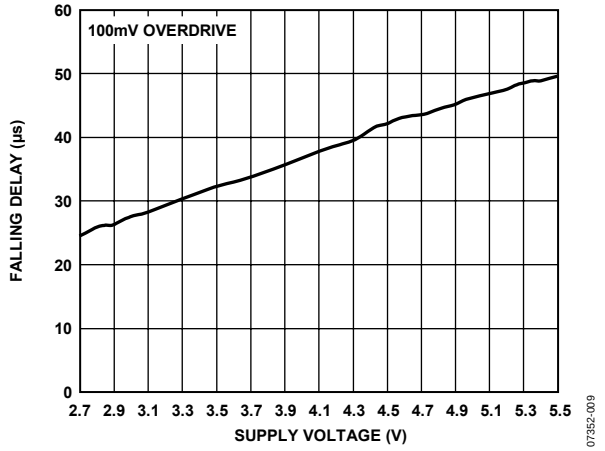


Figure 9. VINx to Output Falling Delay vs. Supply Voltage

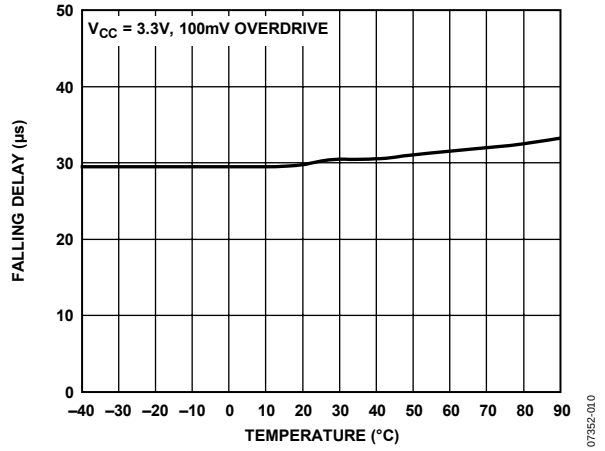


Figure 10. VINx to Output Falling Delay vs. Temperature

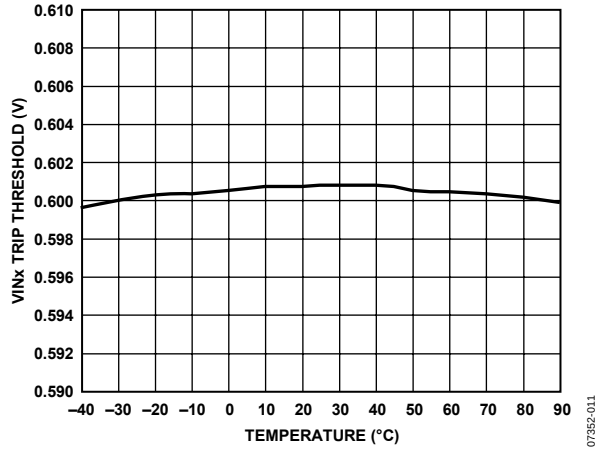


Figure 11. VINx Trip Threshold vs. Temperature

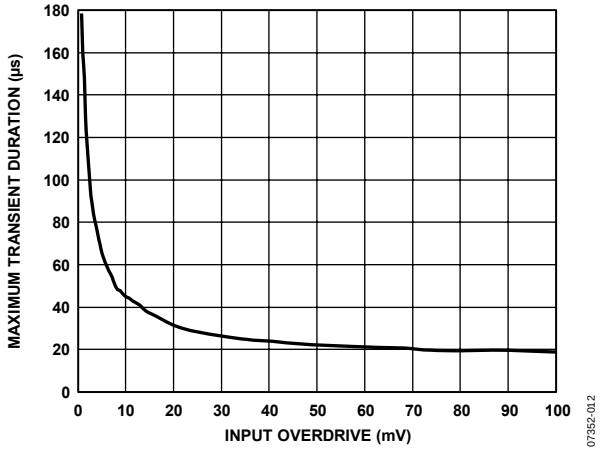


Figure 12. Trip Threshold Maximum Transient Duration vs. Input Overdrive

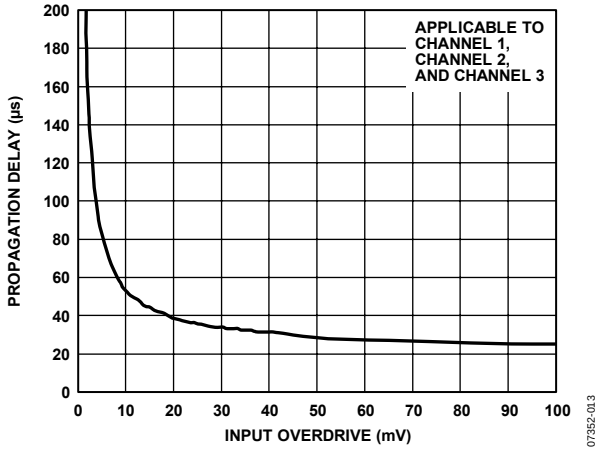


Figure 13. Propagation Delay vs. Input Overdrive

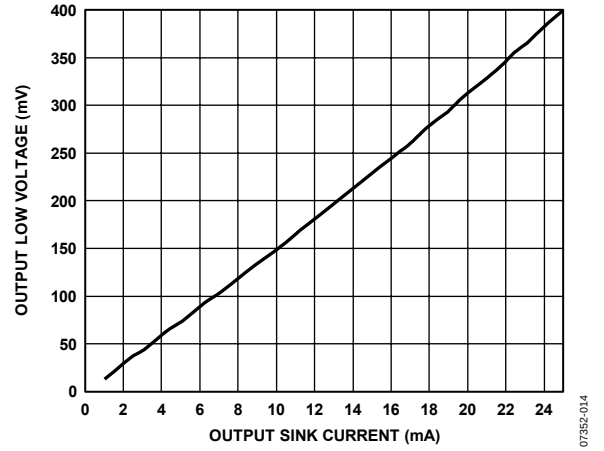


Figure 14. Output Low Voltage vs. Output Sink Current

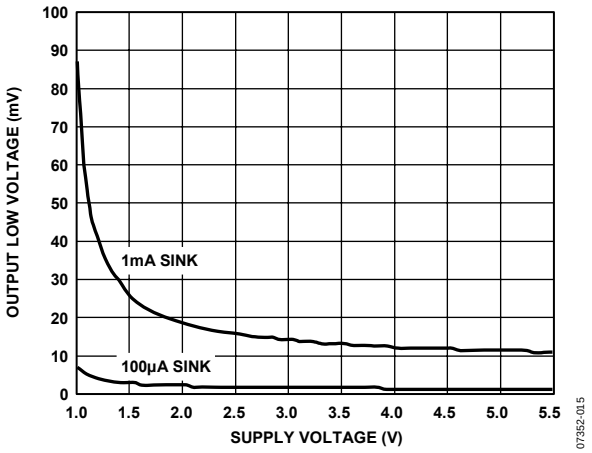


Figure 15. Output Low Voltage vs. Supply Voltage

THEORY OF OPERATION

The ADM1184 is an integrated, 4-channel voltage-monitoring device. A 2.7 V to 5.5 V power supply is required on the VCC pin to power the device.

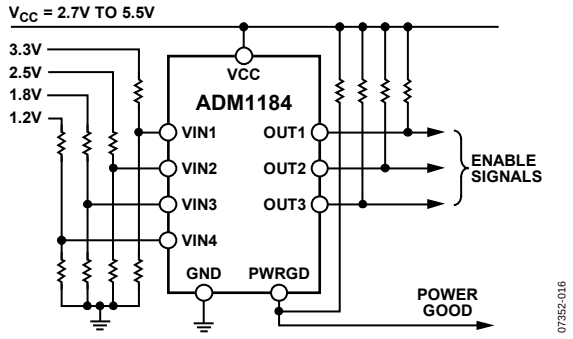


Figure 16. Typical Applications Circuit

INPUT CONFIGURATION

Four precision comparators monitor four voltage rails. Each comparator has a 0.6 V reference with a worst-case accuracy of 0.8%. Resistor networks external to the VIN1, VIN2, VIN3, and VIN4 pins set the trip points for the monitored supply rails.

Typically, the threshold voltage at each of the four adjustable inputs (that is, VIN1, VIN2, VIN3, and VIN4) is 0.6 V. To monitor a voltage greater than 0.6 V, connect a resistor divider network to the circuit as depicted in Figure 17.

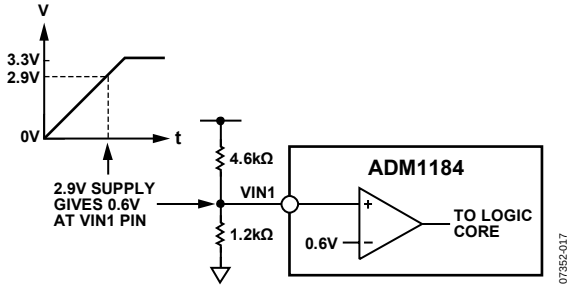


Figure 17. Setting the Undervoltage Threshold

In this example, the VIN1 pin monitors a 3.3 V supply. An external resistor divider scales this voltage down for monitoring at the VIN1 pin. The resistor ratio is chosen so that the VIN1 voltage is 0.6 V when the main voltage rises to the preferred level at startup (a voltage below the nominal 3.3 V level). R1 is 4.6 kΩ and R2 is 1.2 kΩ; therefore, a voltage level of 2.9 V corresponds to 0.6 V on the noninverting input of the first comparator (see Figure 17).

OUTPUT CONFIGURATION

The ADM1184 has four open-drain, active high outputs. Of these outputs, OUT1 to OUT3 can be used to enable power supplies, and PWRGD is a common power-good output.

Output OUT1 to Output OUT3 are dependent on their associated input (that is, VIN1, VIN2, or VIN3). Before the voltage on a VINx input reaches 0.6 V, the corresponding output is switched to ground if there is 1 V on the VCC pin of the ADM1184. When VINx detects 0.6 V, OUTx is asserted after a 30 µs (typical) delay.

When all four monitored supplies exceed 0.6 V, a system power-good signal (PWRGD) is asserted. There is an internal 190 ms (typical) delay associated with the assertion of the PWRGD output. After PWRGD is asserted, if any of the four monitored supplies drops below its programmed threshold, the corresponding OUTx output and the PWRGD output are deasserted. If only the supply monitored by VIN4 drops below its programmed threshold, just the PWRGD output is deasserted.

The ADM1184 functional truth table is shown in Table 5. Note that the functional operation described in Table 5 applies to the operation both before and after the assertion of PWRGD.

Table 5. Functional Truth Table

VIN1	VIN2	VIN3	VIN4	OUT1	OUT2	OUT3	PWRGD
0[1]	0	0	0	Low	Low	Low	Low
0	0	0	1[2]	Low	Low	Low	Low
0	0	1	0	Low	Low	High	Low
0	0	1	1	Low	Low	High	Low
0	1	0	0	Low	High	Low	Low
0	1	0	1	Low	High	Low	Low
0	1	1	0	Low	High	High	Low
0	1	1	1	Low	High	High	Low
1	0	0	0	High	Low	Low	Low
1	0	0	1	High	Low	Low	Low
1	0	1	0	High	Low	High	Low
1	0	1	1	High	Low	High	Low
1	1	0	0	High	High	Low	Low
1	1	0	1	High	High	Low	Low
1	1	1	0	High	High	High	Low
1	1	1	1	High	High	High	High

[1] $<V_{TH}$ = 0.
[2] $>V_{TH}$ = 1.

Figure 18 and Figure 19 show waveforms that illustrate the behavior of the ADM1184.

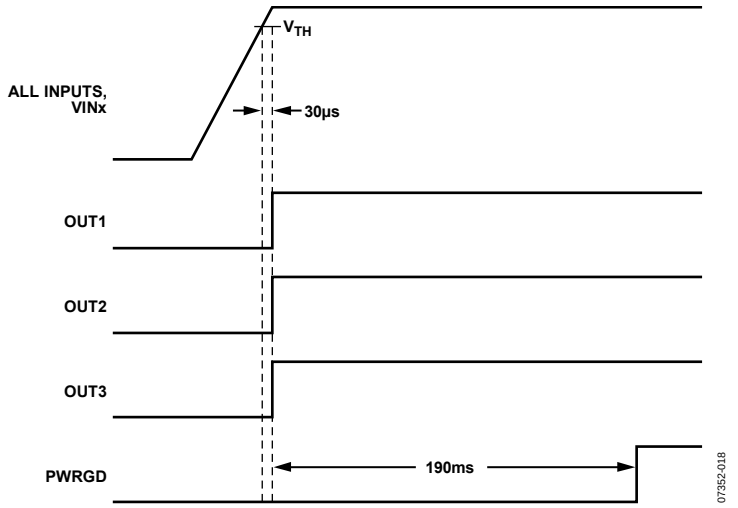


Figure 18. Power-Up Waveforms

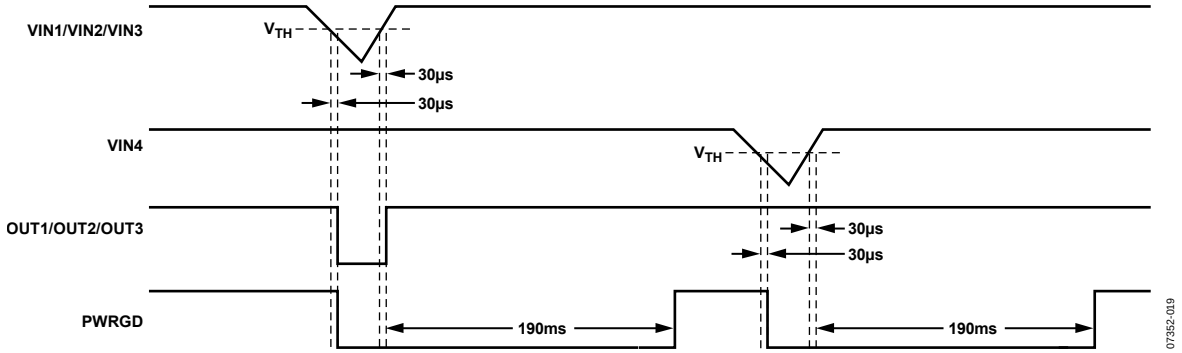


Figure 19. Waveforms Showing Reaction to a Temporary Low Glitch on VIN1, VIN2, VIN3, or VIN4

VOLTAGE MONITORING AND SEQUENCING APPLICATION

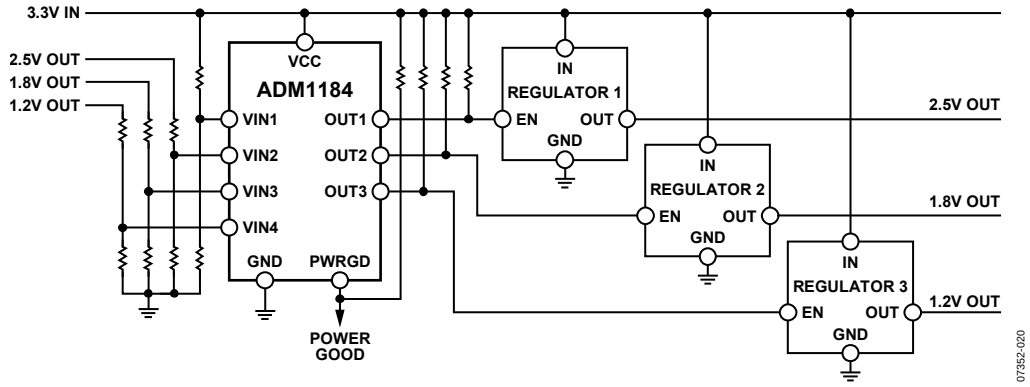


Figure 20. Voltage-Monitoring and Sequencing Application Diagram

Figure 20 depicts an application in which the ADM1184 monitors four separate voltage rails, turns on three regulators in a sequence, and generates a power-good signal to turn on a controller when all power supplies are up and stable.

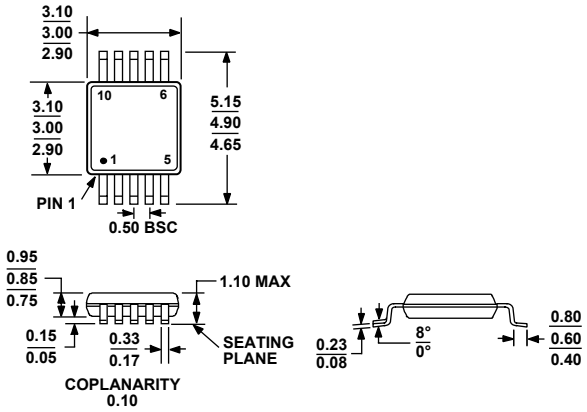
The main supply, in this case 3.3 V, powers up the device via the VCC pin. The VIN1 pin monitors the main 3.3 V supply. In this example application, OUT1 is connected to the enable pin of a regulator. Before the voltage on VIN1 reaches 0.6 V, this output is switched to ground, disabling Regulator 1.

When the main system voltage reaches 2.9 V, VIN1 detects 0.6 V. This causes OUT1 to assert, which drives the enable pin of Regulator 1 high, thus turning on its output.

The 2.5 V output of this regulator begins to rise and is detected by input Pin VIN2. When VIN2 detects the 2.5 V rail rising above its voltage threshold point, it asserts OUT2, which turns on Regulator 2. The same scheme is implemented with the other input and output pins. Every rail that is turned on via an output pin, OUTx, is monitored via an input pin, VIN(x + 1).

When all four monitored supplies are above their programmed threshold levels PWRGD asserts after a 190 ms (typical) delay.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 21. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADM1184ARMZ[1]	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MB0
ADM1184ARMZ-REEL7[1]	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	MB0

[1] Z = RoHS Compliant Part.

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