

# NTMD6N02R2

## Power MOSFET 6.0 Amps, 20 Volts

### N-Channel Enhancement Mode Dual SO-8 Package

#### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SOIC-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SOIC-8 Mounting Information Provided
- Pb-Free Package is Available

#### Applications

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery-Powered Products, for example, Computers, Printers, Cellular and Cordless Telephones and PCMCIA Cards

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	20	V
Drain-to-Gate Voltage ( $R_{GS} = 1.0\ \text{M}\Omega$ )	$V_{DGR}$	20	V
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 12$	V
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	2.0	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	6.5	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	5.5	A
Pulsed Drain Current (Note 4)	$I_{DM}$	50	A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	102	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.22	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	5.07	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	4.07	A
Pulsed Drain Current (Note 4)	$I_{DM}$	40	A
Thermal Resistance Junction-to-Ambient (Note 3)	$R_{\theta JA}$	172	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	0.73	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	3.92	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	3.14	A
Pulsed Drain Current (Note 4)	$I_{DM}$	30	A

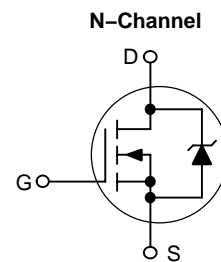
1. Mounted onto a 2 in square FR-4 Board (1 in sq. 2 oz. Cu 0.06 in thick single sided),  $t < 10$  seconds.
2. Mounted onto a 2 in square FR-4 Board (1 in sq. 2 oz. Cu 0.06 in thick single sided),  $t =$  steady state.
3. Minimum FR-4 or G-10 PCB,  $t =$  steady state.
4. Pulse Test: Pulse Width = 10  $\mu\text{s}$ , Duty Cycle = 2%.



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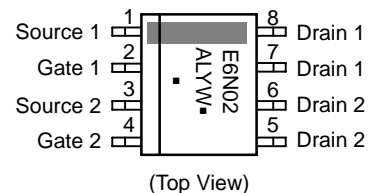
<http://onsemi.com>

$V_{DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
20 V	35 m $\Omega$ @ $V_{GS} = 4.5$ V	6.0 A



SOIC-8  
CASE 751  
STYLE 11

#### MARKING DIAGRAM & PIN ASSIGNMENT



E6N02 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping†
NTMD6N02R2	SOIC-8	2500/Tape & Reel
NTMD6N02R2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Rating	Symbol	Value	Unit
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 20\text{ Vdc}$ , $V_{GS} = 5.0\text{ Vdc}$ , Peak $I_L = 6.0\text{ Apk}$ , $L = 20\text{ mH}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	360	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	$T_L$	260	$^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\ \mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	20 –	– 19.2	– –	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ )	$I_{DSS}$	– –	– –	1.0 10	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = +12\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	100	nAdc
Gate-Body Leakage Current ( $V_{GS} = -12\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	–	–	-100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{Adc}$ ) Temperature Coefficient (Negative)	$V_{GS(th)}$	0.6 –	0.9 -3.0	1.2 –	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-State Resistance ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 6.0\text{ Adc}$ ) ( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 4.0\text{ Adc}$ ) ( $V_{GS} = 2.7\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ ) ( $V_{GS} = 2.5\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )	$R_{DS(on)}$	– – – –	0.028 0.028 0.033 0.035	0.035 0.043 0.048 0.049	$\Omega$
Forward Transconductance ( $V_{DS} = 12\text{ Vdc}$ , $I_D = 3.0\text{ Adc}$ )	$g_{FS}$	–	10	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 16\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	–	785	1100	pF
Output Capacitance		$C_{oss}$	–	260	450	
Reverse Transfer Capacitance		$C_{rss}$	–	75	180	

### SWITCHING CHARACTERISTICS (Notes 6 and 7)

Turn-On Delay Time	$(V_{DD} = 16\text{ Vdc}$ , $I_D = 6.0\text{ Adc}$ , $V_{GS} = 4.5\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	–	12	20	ns
Rise Time		$t_r$	–	50	90	
Turn-Off Delay Time		$t_{d(off)}$	–	45	75	
Fall Time		$t_f$	–	80	130	
Turn-On Delay Time	$(V_{DD} = 16\text{ Vdc}$ , $I_D = 4.0\text{ Adc}$ , $V_{GS} = 4.5\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	–	11	18	ns
Rise Time		$t_r$	–	35	65	
Turn-Off Delay Time		$t_{d(off)}$	–	45	75	
Fall Time		$t_f$	–	60	110	
Total Gate Charge	$(V_{DS} = 16\text{ Vdc}$ , $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 6.0\text{ Adc}$ )	$Q_{tot}$	–	12	20	nC
Gate-Source Charge		$Q_{gs}$	–	1.5	–	
Gate-Drain Charge		$Q_{gd}$	–	4.0	–	

5. Handling precautions to protect against electrostatic discharge is mandatory
6. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

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## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (continued) (Note 8)

Characteristic		Symbol	Min	Typ	Max	Unit
<b>BODY-DRAIN DIODE RATINGS</b> (Note 9)						
Diode Forward On-Voltage	( $I_S = 4.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc}$ )	$V_{SD}$	-	0.83	1.1	Vdc
	( $I_S = 6.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc}$ )		-	0.88	1.2	
	( $I_S = 6.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^\circ\text{C}$ )		-	0.75	-	
Reverse Recovery Time	( $I_S = 6.0 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$ $di_S/dt = 100 \text{ A}/\mu\text{s}$ )	$t_{rr}$	-	30	-	ns
		$t_a$	-	15	-	
		$t_b$	-	15	-	
Reverse Recovery Stored Charge		$Q_{RR}$	-	0.02	-	$\mu\text{C}$

8. Handling precautions to protect against electrostatic discharge is mandatory.

9. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.

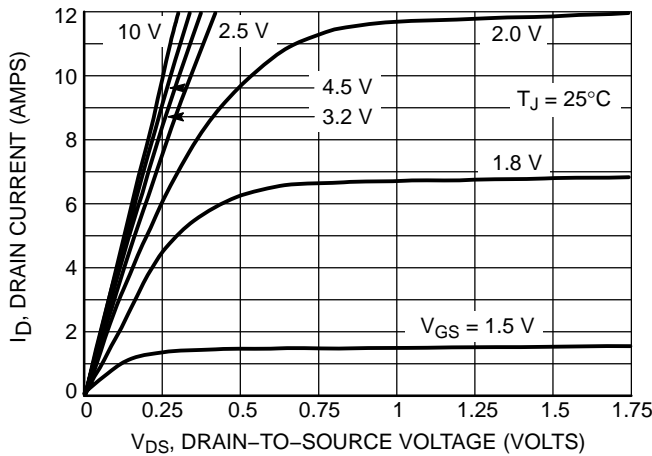


Figure 1. On-Region Characteristics

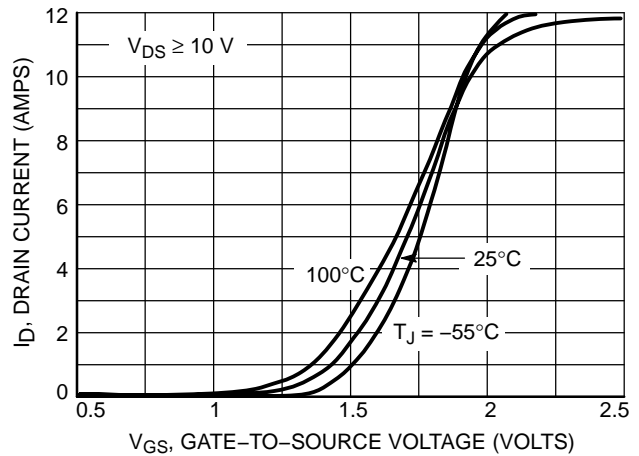


Figure 2. Transfer Characteristics

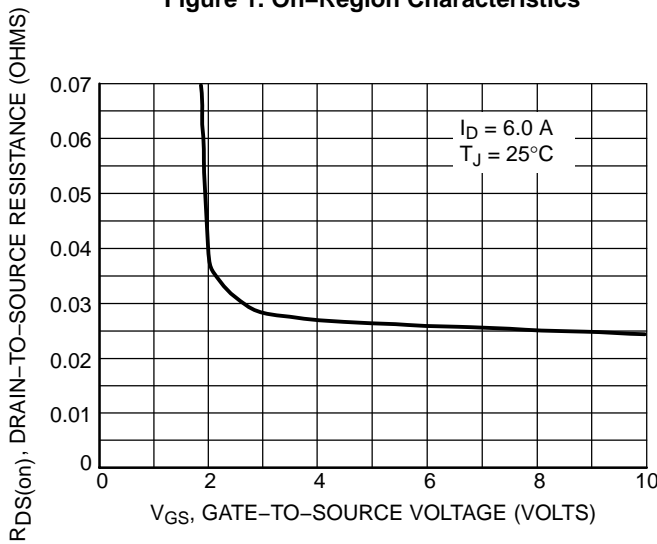


Figure 3. On-Resistance versus Gate-to-Source Voltage

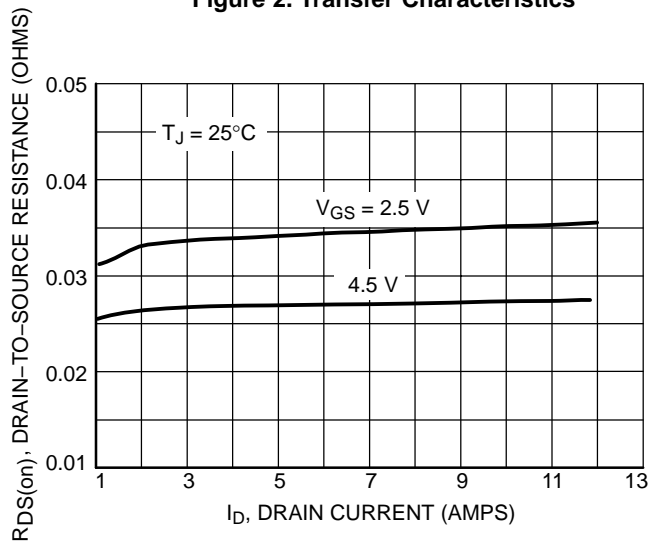
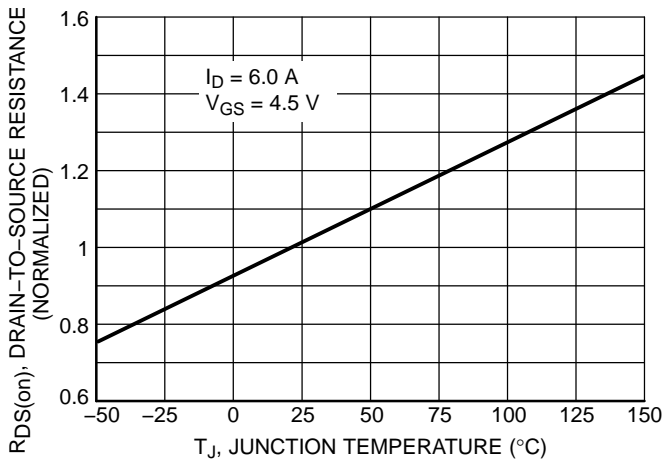
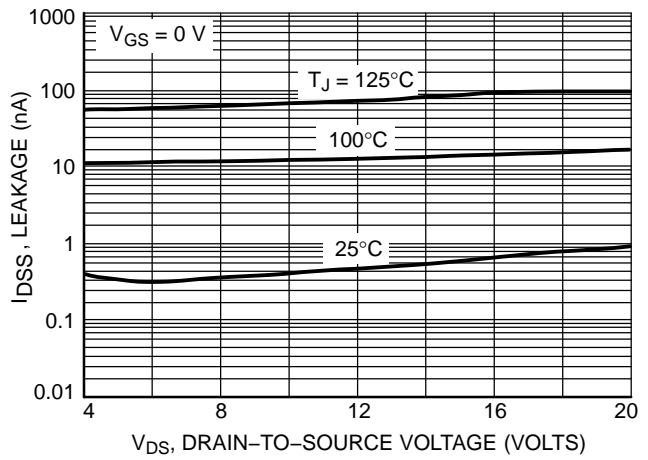


Figure 4. On-Resistance versus Drain Current and Gate Voltage

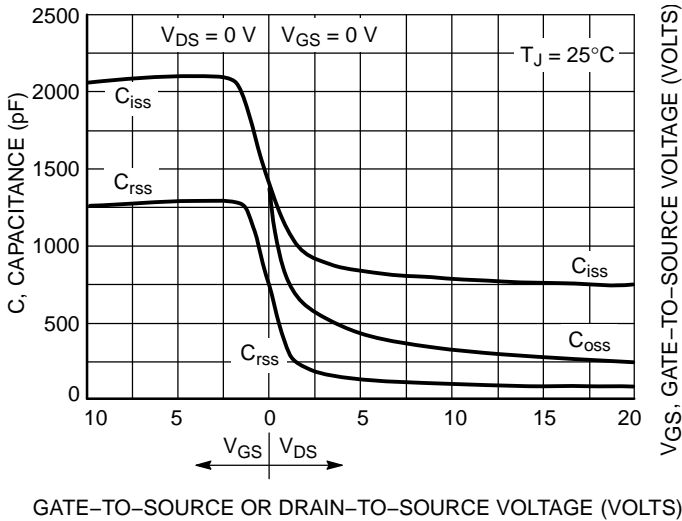
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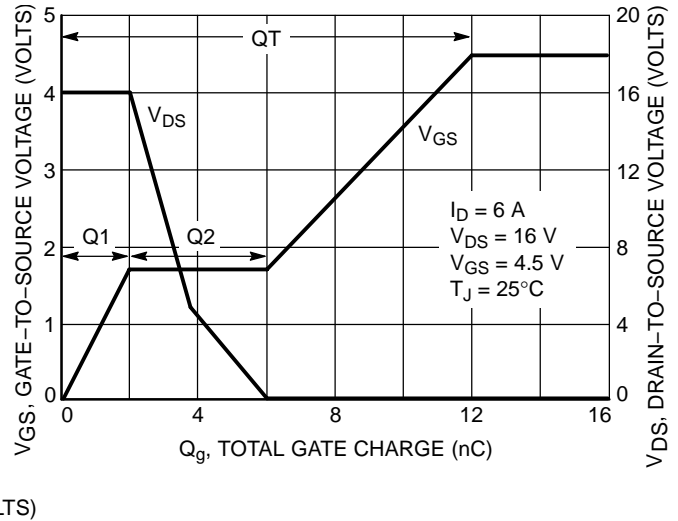
**Figure 5. On-Resistance Variation with Temperature**



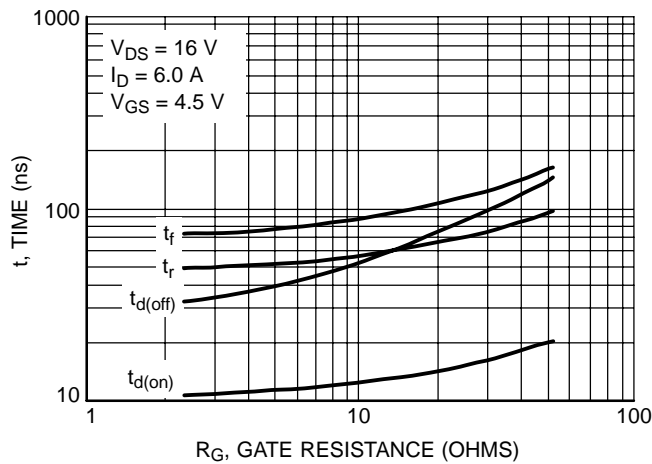
**Figure 6. Drain-To-Source Leakage Current versus Voltage**



**Figure 7. Capacitance Variation**



**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

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## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

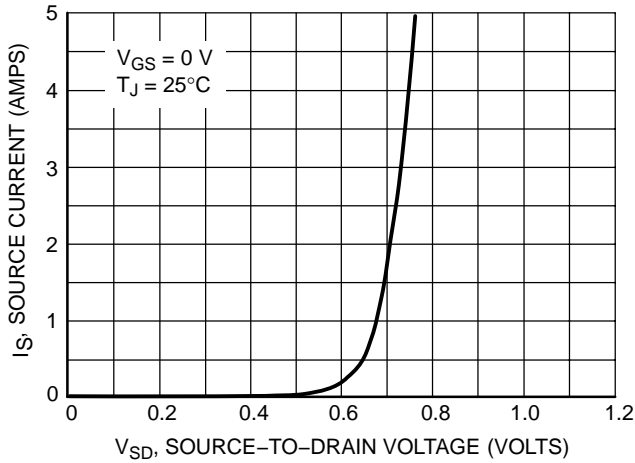


Figure 10. Diode Forward Voltage versus Current

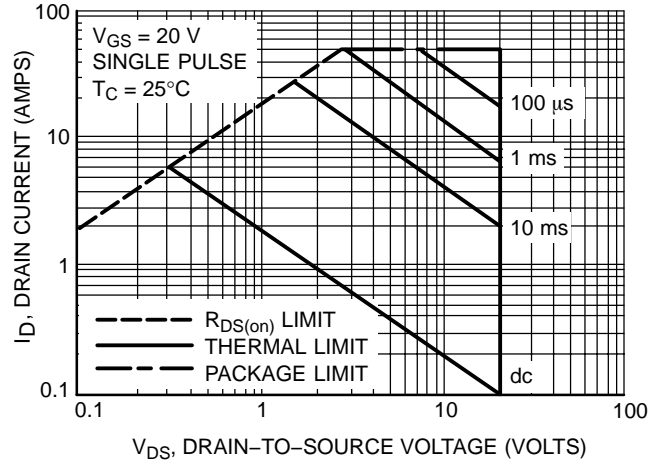


Figure 11. Maximum Rated Forward Biased Safe Operating Area

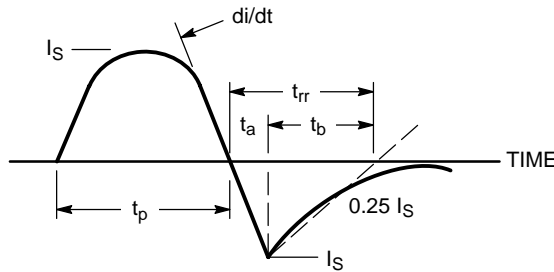


Figure 12. Diode Reverse Recovery Waveform

## TYPICAL ELECTRICAL CHARACTERISTICS

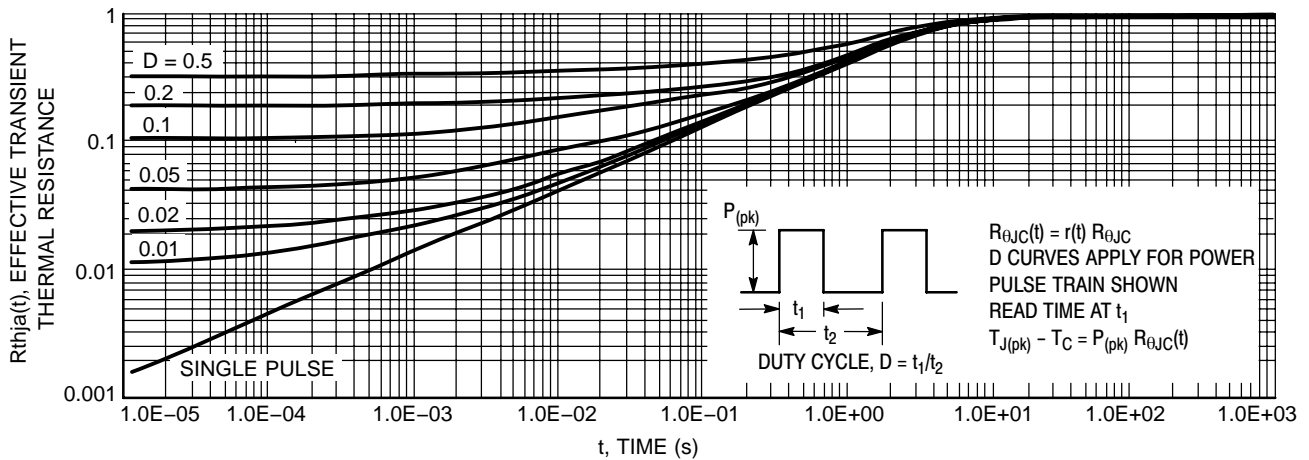
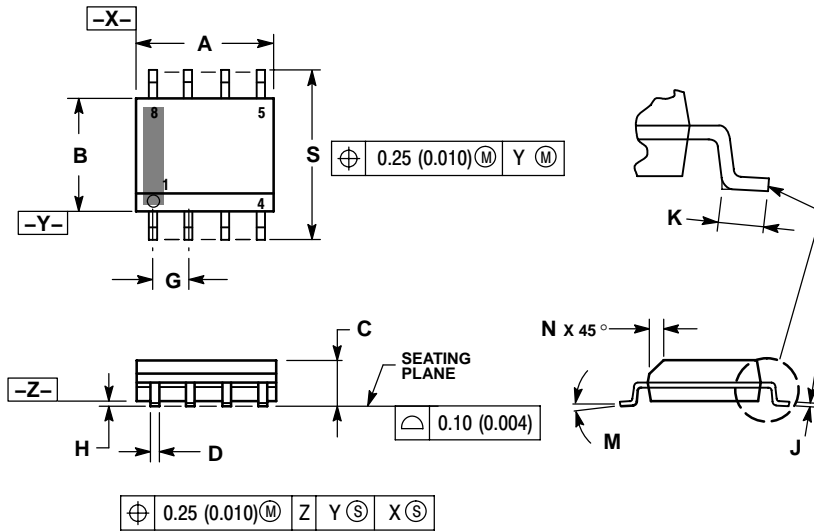


Figure 13. Thermal Response

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## PACKAGE DIMENSIONS

SOIC-8  
CASE 751-07  
ISSUE AG



**NOTES:**

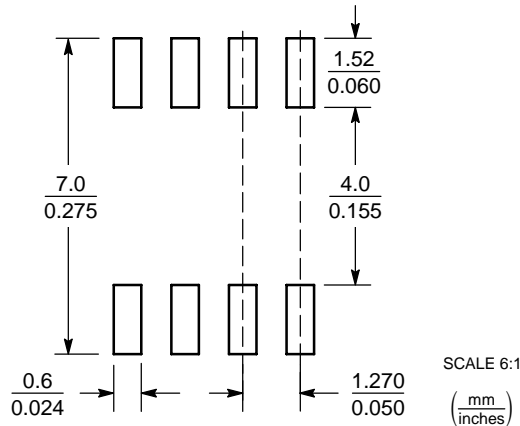
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

**STYLE 11:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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